



GPLB3X Programming Guide & Development System User's Guide

V1.8 09/18/2008

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Revision History

Revision	Date	By	Remark
V1.8	09/18/2008	Frank Kung	<ol style="list-style-type: none"> 1. Modify LCD frame rate table of GPLB33A and GPLB33B : \$25.3~\$24.2 to \$25.3~\$25.2. P.15 2. Modify GPLB33B LCD dots : 832 to 768. P.23 3. Modify Low Voltage Detector of GPLB37, 39 : 2.9V~2.2V to 2.9V~2.4V. P.27, 28 4. Modify P_13H_Ch0_PWM_DAC_Output description : \$17H to \$13H. 5. Modify P_17H_Ch1_PWM_DAC_Output description : \$13H to \$17H. 6. Add GPLB30B EV Chip information.
V1.7	06/24/2008	Frank Kung	<ol style="list-style-type: none"> 1. Add key scan function notice. 2. Modify key scan program example.
V1.6	11/19/2007	Jason Chen	<ol style="list-style-type: none"> 1. Modify SPI phase = 1 2. Modify SDI shared with PortA6 , SDO shared with PortA.5 3. Add P_3008H Note
V1.5	05/28/2007	Frank Kung	<ol style="list-style-type: none"> 1. Modify GPLB33B ROM Size, VLCD Level and LCD frame rate. 2. Add PD shared com/segment description P.13 3. Modify P_31H_Serial_SRAM_Addr1 condition P.89 4. Modify SPI Master Mode Structure P.105 5. Add reset flag description P.116 6. Add reset flag in assembly file P.119 7. Delete GPLB33A voltage regulator of mask option P.121 8. Add GPLB33B mask option P.122 9. Modify GPLB33A Register Reset Value to GPLB33 P.128
V1.4	05/02/2007	Frank Kung	<ol style="list-style-type: none"> 1. Modify GPLB33B ROM Size 、VLCD Level and LCD frame rate 2. Add PD shared com/segment description P.12 3. Modify condition of P_31H_Serial_SRAM_Addr1 P.94 4. Modify SPI Master Mode Structure P.111 5. Modify reset flag description P.123
V1.3	01/09/2007	Jason Chen	<ol style="list-style-type: none"> 1. Add programming check list in section 1.1. 2. Add register reset value in section 27. 3. Section 2.3.10 GPLB39 only PWM output. 4. P_3034H_LB39B_EV_Chip_Ctrl : regulator default enable. 5. LCD FRAME RATE. 6. Del GPLB3X series selection guide. 7. Add GPLB33B. 8. Add GPLB3X EV vs. real IC difference. 9. Del SPR4096 Bus flash.
V1.2	05/25/2006	Jason Chen	<ol style="list-style-type: none"> 1. Modify note of memory map in section 3.3. 2. Modify the program example in section 11.4. 3. Modify the program example in section 14.8. 4. Add the note of LVR to section 19.

Revision	Date	By	Remark
V1.1	12/23/2005	Jason Chen	<ol style="list-style-type: none"> 1. Add descriptions to shared PortC [0,1] with SCK, SDA of SSRAM. 2. Add descriptions to shared PortC [4,5] with Ext-I, Ext-ck for all bodies. 3. Add descriptions to shared PortA [7,5] with SCK, SDI and SDO of SPI for GPLB35A, GPLB36A, GPLB39A and GPLB39B. 4. Modify the "296 bytes dedicated LCD RAM" in section 2.4.5. 5. Modify the "600 bytes dedicated LCD RAM" and "32-level contrast control (2.45V ~ 8.21V, 1/5 - 1/8 bias)" in section 2.4.6 and 2.4.7. 6. Modify the "32-level contrast control (2.45V ~ 8.05V, 1/4 - 1/8 bias)" in section 2.4.9. 7. Add the "play tone setting" to section 8.1 and 8.2. 8. Modify the "LCD Driver Feature Table for GPLB3X" in section 10.1. 9. Add the note3 and note7 to section 10.8 for descriptions of P_2EH_LCD_CTL1 register VCIB0~VCIB2(bit2~4). 10. Remove the "28.APPENDIX B. BLOCK DIAGRAM", "31.5.Approval Form of 31.DIFFERENCES BETWEEN EMU CHIP AND REAL CHIP(GPLB32A)", "32.3~32.7 of 32.EMU BOARD", "33.PIGGYBACK", "34.GPLB3X EMU BOARD SCHEMATICS", "35.GPLB35 PIGGYBACK SCHEMATICS", and "36.SPBA01B SCHEMATICS V1.2". 11. Add the hardware: "1.GPLB3X EMU board = GPLB30 /GPLB35 /GPLB39 EMU BOARD.", "2.GPLB30 EMU board : please refer to GPLB3X Development Board User Manual v1.0 for more details.", "3.GPLB35 EMU board : please refer to GPLB34/GPLB35 EV Board User's Guide v1.0 for more details." and "4.GPLB39 EMU board : please refer to GPLB39 EV Board User's Guide v1.0 for more details." to section 29.2.
V1.0	02/14/2005	Tony Hsu	<p>Original</p> <p>Note: The GPLB3X programming guide v1.0 is a continued version of SPLB3X programming guide v3.6.</p>

1. Important Notice Before Writing Your Program

● Confirmation Sheet

It is highly recommended programmers to obtain a copy of appropriate confirmation sheet before writing program. The confirmation sheet, a requisite document before placing orders, contains useful information and checklist to help programmers avoiding mistakes during program development. Due to the possible changes may be made in the confirmation sheet occasionally, an up-to-date confirmation sheet can be downloaded from GENERALPLUS web site at <http://www.generalplus.com>.

1.1. Programming Check List

1. When system powers on, LCD control port and buffer must be initialized. Otherwise, the data of LCD driver will be randomly generated.
2. When UART is applied, all configurations in \$19 should be set up again and \$19.5 must be set to "0" after reset operation (\$19.5=1).
3. Disable LCD Pump Control (\$25.7="0") before entering standby mode.
4. When an I/O is optioned to a segment/common, the I/O pin (used as segment/common) must be masked off while reading the I/O port.
5. When PortA is used for key-scan input port (pins), all pins for key-scan input must be configured as pull-high state.
6. PWM Ch0/Ch1 frequency is determined by Timer0/Timer1.
7. In DAC mode, the \$12.7/\$16.7 must be set to "0" after end of audio play or before sleep entrance. Otherwise, it will cause a 5mA current consumption once the \$12.7/16.7 is set to "1" even though the DAC output (\$13/\$17) ramps down to 0.
8. The following test program area and test program vectors are reserved for GENERALPLUS. The user's program or data must not be in these ROM areas.
 - Test Program Area : CPU view: \$C000 ~ \$C7FF
ROM area: \$4000 ~ \$47FF
 - Test Program Vector : CPU View: FFF2 ~ FFF7
ROM View: 7FF2 ~ 7FF7
9. CPU stack pointer must be reset after system power-on and wake-up.
10. All RAM must be initialized after power on.
11. Timer content must be initialized before timer interrupt is enabled.
12. Do not enable interrupt before initializing RAM.
13. The instructions of "SEI" and "CLI" must be removed from the IRQ and NMI service routines.
14. Sleep port must be cleared and re-initialized before entering sleep mode.

15. The used RAM not over the stack reserved area.
16. Non-used I/O ports should be masked off (for input process).
17. When 32KHz X'TAL and LVR mask options are both enabled, it is prohibited that CPU and 32KHz clock stop at the same time in sleep mode. That is, DON'T stop the 32KHz RTC clock when in sleep mode. Otherwise an unexpected reset may occur when CPU wakes up from sleep mode.

1.2. Differences of All Body can be Simulated on GPLB30BEV

	Working voltage	ROM	RAM	I/O Max	com* seg	Bias	Duty	Dots	AUD	SIF	BMI	UR
GPLB30	2.4-5.5	96K	2752+140	29	16*70	1/5	1/16	1120	PWM	V	V	V
GPLB31	2.4-5.5	256K	4288+296	29	32*74	1/5 1/6	1/32	2368	PWM	V	V	V
GPLB32	2.4-5.5	512K	1216+296	28	16*74 32*64	1/5 1/6	1/16 1/32	2048	DAC PWM	V	X	V
GPLB33A	2.4-5.5	64K	1216+104	24	16*52	1/5	1/16	832	PWM	V	X	V
GPLB33B	2.4-3.6	96K	1024+96	24	16*48	1/3 1/4 1/5	1/4 1/8 1/16	768	PWM	X	X	X
GPLB37	2.4-5.5	256K	1216+296	28	16*74 32*64	1/5 1/6	1/16 1/32	2048	DAC PWM	V	X	V

● PA shared segment

	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
LB30	S67	S68	S69	-	-	-	-	-
LB31	S69	S70	S71	S72	S73	-	-	-
LB32/37	S62	S63	-	-	-	-	-	-
LB33A	S51	-	-	-	-	-	-	-
LB33B	-	-	-	-	-	-	-	-

● PB shared com/segment

	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
LB30	S57	S58	S59	S60	S61	S62	S63	S64
LB31	-	-	-	-	-	-	-	-
LB32/37	X	X	C16/S64	C17/S65	C18/S66	C19/S67	C20/S68	C21/S69
LB33A	S39	S40	S41	S42	S43	S44	S45	S46
LB33B	S34	S35	S36	S37	S38	S39	S40	S41

● PC shared com/segment

	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
LB30	S53	S54	S55	S56	S65	S66	-	-
LB31	S65	S66	S67	S68	-	-	-	-
LB32/37	C22/S70	C23/S71	C24/S72	C25/S73	-	-	S60	S61
LB33A	S47	S48	S49	S50	-	-	-	-
LB33B	S42	S43	S44	S45	S46	S47	-	-

● PD sharing with com/segment

	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
LB30	x	x	x	S48	S49	S50	S51	S52
LB31	x	x	x	C27	C28	C29	C30	C31
LB32/37	x	x	C26	C27	C28	C29	C30	C31
LB33A	x	x	x	x	x	x	x	x
LB33B	x	x	x	x	x	x	x	x

“ - “ : not shared

“ x ” : not used

1.3. Differences of All Body can be Simulated on GPLB35EV

	ROM	RAM	com* seg	Bias	Duty	Dots	SPI
GPLB34	1M	2752+296	32X74	1/5 1/6	1/16 1/32	2368	X
GPLB35	1M	2752+600	32X100 36X96 48X84	1/5 1/6 1/7 1/8	1/16 1/32 1/36 1/48	4032	V
GPLB36	512K	2752+600	32X100 36X96 48X84	1/5 1/6 1/7 1/8	1/16 1/32 1/36 1/48	4032	V

● PA shared pin

	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
LB34	-	-	-	-	-	-	-	-
LB35	SPI_SCK	SPI_DI	SPI_DO	-	-	-	-	-
LB36	SPI_SCK	SPI_DI	SPI_DO	-	-	-	-	-

“ - “ : not shared

1.4. Differences between GPLB33A and GPLB33B

1. Below is the VLCD contrast table of GPLB33A and GPLB33B.

\$26.4 ~ \$26.0					GPLB33A	GPLB33B
b4	b3	b2	b1	b0	1/5 bias	1/3 bias 1/4 bias 1/5 bias
0	0	0	0	0	2.45	-
0	0	0	0	1	2.56	-
0	0	0	1	0	2.66	-
0	0	0	1	1	2.77	-
0	0	1	0	0	2.88	-
0	0	1	0	1	2.98	2.98
0	0	1	1	0	3.09	3.09
0	0	1	1	1	3.19	3.19
0	1	0	0	0	3.30	3.30
0	1	0	0	1	3.41	3.41
0	1	0	1	0	3.51	3.51
0	1	0	1	1	3.62	3.62
0	1	1	0	0	3.73	3.73
0	1	1	0	1	3.83	3.83
0	1	1	1	0	3.94	3.94
0	1	1	1	1	4.05	4.05
1	0	0	0	0	4.15	4.15
1	0	0	0	1	4.26	4.26
1	0	0	1	0	4.37	4.37
1	0	0	1	1	4.47	4.47
1	0	1	0	0	4.58	4.58
1	0	1	0	1	4.68	4.68
1	0	1	1	0	4.79	4.79
1	0	1	1	1	4.90	4.90
1	1	0	0	0	5.00	5.00
1	1	0	0	1	5.11	5.11
1	1	0	1	0	5.22	5.22
1	1	0	1	1	5.32	5.32
1	1	1	0	0	5.43	5.43
1	1	1	0	1	5.54	5.54
1	1	1	1	0	5.64	5.64
1	1	1	1	1	5.75	5.75

2. The following table is the duty setting of GPLB33A and GPLB33B.

\$24.7~\$24.6		GPLB33A	GPLB33B
b7	b6		
0	0	1/16 duty	1/16 duty
0	1	X	1/4 duty
1	0	1/16 duty	1/16 duty
1	1	X	1/8 duty

3. The following table is the bias setting of GPLB33A and GPLB33B.

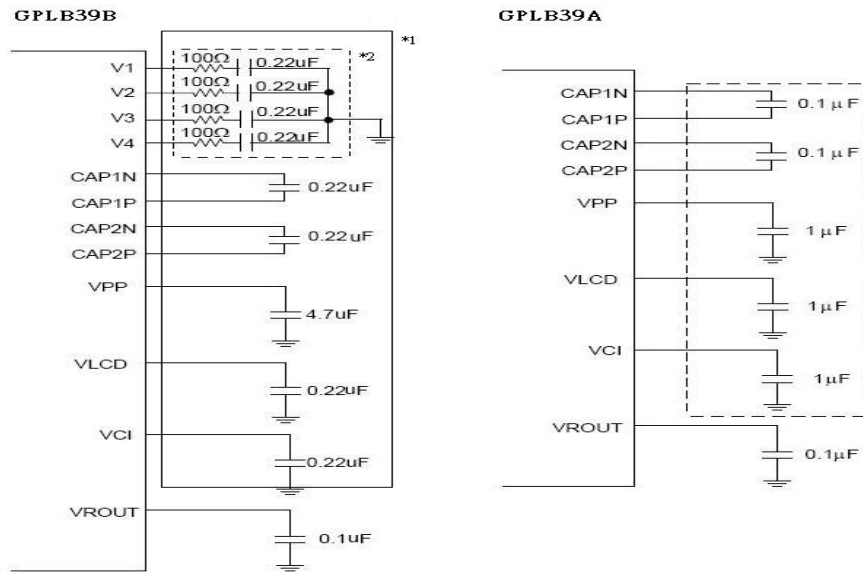
\$24.5~\$24.4		GPLB33A	GPLB33B
b5	b4		
0	0	1/5 bias	1/5 bias
0	1	X	1/5 bias
1	0	X	1/3 bias
1	1	X	1/4 bias

4. The following table is the LCD frame rate setting of GPLB33A and GPLB33B.

\$25.3~\$25.2		GPLB33A	GPLB33B
b3	b2		
0	0	X	64Hz
0	1		68Hz
1	0	Only 64Hz	73Hz
1	1		79Hz

1.5. Differences between GPLB39A and GPLB39B

1. GPLB39B can be simulated on GPLB39EV. GPLB39A just can simulate function on GPLB39EV.
2. Compared to GPLB39A, GPLB39B has additional pins V1 V2 V3 V4 (108~111) and VDD VSS (214, 1). GPLB39B has better display quality than GPLB39A. The VLCD contrast level of GPLB39B is also different.
3. V1/V2/V3/V4 pins should be connected 0.22uF capacitors to VSS.



Note*1: The suggested capacitor values of GPLB39B are different from GPLB39A. These capacitor values are for design guidance only. Different resistor/capacitor values may be required for different LCD panel connected.

Note*2: Usually, these resistors/capacitors may not be needed when large LCD panel is connected.

4. VDD(214) is positive supply for SEG/COM only, and VSS(1) is ground reference for SEG/COM only. These two pins must be bonded for proper operation.
5. R_{osc} vs. F_{ROSC}

R_{osc} (Kohm)	GPLB39A	GPLB39B
	Typical(MHz)	Typical(MHz)
36	7.04	7.48
43	5.97	6.47
47	5.42	5.96
56	4.74	5.17
68	3.99	4.33
75	3.70	3.98
100	2.86	3.05
150	1.94	2.07
200	1.49	1.59
240	1.25	1.31
300	1.02	1.05
360	0.85	0.89

R_{32K} (Kohm)	GPLB39A	GPLB39B
	Typical(KHz)	Typical(KHz)
680	30.3	33.3

6. The below is the VLCD contrast table of GPLB39A and GPLB39B.

					GPLB39A			GPLB39B		
\$26.4 ~ \$26.0					1/5 bias	1/6, 1/7 bias	1/8, 1/9 bias	1/5 bias	1/6, 1/7 bias	1/8, 1/9 bias
b4	b3	b2	b1	b0						
0	0	0	0	0	2.45	2.95	3.53	4.400	5.28	6.20
0	0	0	0	1	2.56	3.08	3.67	4.420	5.33	6.26
0	0	0	1	0	2.66	3.20	3.83	4.840	5.38	6.32
0	0	0	1	1	2.77	3.33	3.97	4.526	5.43	6.38
0	0	1	0	0	2.88	3.45	4.12	4.568	5.48	6.44
0	0	1	0	1	2.98	3.58	4.25	4.610	5.53	6.50
0	0	1	1	0	3.09	3.71	4.43	4.652	5.58	6.56
0	0	1	1	1	3.19	3.83	4.56	4.694	5.63	6.62
0	1	0	0	0	3.30	3.96	4.71	4.736	5.68	6.68
0	1	0	0	1	3.41	4.08	4.86	4.778	5.73	6.74
0	1	0	1	0	3.51	4.21	5.03	4.820	5.78	6.80
0	1	0	1	1	3.62	4.33	5.18	4.862	5.83	6.86
0	1	1	0	0	3.73	4.46	5.33	4.904	5.88	6.92
0	1	1	0	1	3.83	4.59	5.47	4.946	5.93	6.98
0	1	1	1	0	3.94	4.71	5.63	4.988	5.98	7.04
0	1	1	1	1	4.05	4.84	5.77	5.030	6.03	7.10
1	0	0	0	0	4.15	4.96	5.92	5.072	6.08	7.16
1	0	0	0	1	4.26	5.09	6.08	5.114	6.13	7.22
1	0	0	1	0	4.37	5.21	6.23	5.156	6.18	7.28
1	0	0	1	1	4.47	5.34	6.38	5.198	6.23	7.34
1	0	1	0	0	4.58	5.47	6.54	5.240	6.28	7.40
1	0	1	0	1	4.68	5.59	6.68	5.282	6.33	7.46
1	0	1	1	0	4.79	5.72	6.81	5.324	6.38	7.52
1	0	1	1	1	4.9	5.84	6.98	5.366	6.43	7.58
1	1	0	0	0	5.00	5.97	7.13	5.408	6.48	7.64
1	1	0	0	1	5.11	6.10	7.29	5.450	6.53	7.70
1	1	0	1	0	5.22	6.22	7.43	5.492	6.58	7.76
1	1	0	1	1	5.32	6.35	7.60	5.534	6.63	7.82
1	1	1	0	0	5.43	6.47	7.75	5.576	6.68	7.88
1	1	1	0	1	5.54	6.60	7.91	5.618	6.73	7.94
1	1	1	1	0	5.64	6.72	8.05	5.660	6.78	8.00
1	1	1	1	1	5.75	6.85	8.21	5.702	6.83	8.06

GPLB3X Programming Guide

2. Introduction

2.1. General Description

The GPLB3X, an 8-bit CMOS microprocessor with full 6502 compatible instruction, offers 1024/1216/2752/4288/8128 bytes working RAM, 64K/96K/256K/512K/1M/2M bytes of ROM, up to 29 I/Os, interrupt/wakeup controller, UART for serial communication, serial SRAM interface, SPI interface and Bus memory interface for memory expansion, and automatic display controller/driver for LCD.

A PWM or DAC option is available among the GPLB3X series. Attractive sound effects can easily be generated. Its large ROM area can be used to store both program and audio data. The built-in UART speeds up data transmission between two chips. Furthermore, a SLEEP (power-down) feature is also built-in to reduce power consumption. The GPLB3X is designed with GENERALPLUS state-of-the-art technology to fulfill LCD application requirements, especially handheld products.

2.2. Application Field

- Handheld game
- Scientific calculator
- Talking calculator, Talking clock
- Talking instrument controller
- Data bank
- Dictionary
- Translator

2.3. Features

2.3.1. GPLB30

- 8-bit micro-processor
- **2752 bytes SRAM**
- **96K bytes ROM**
- Operating voltage: 2.4V - 3.6V, 3.6V - 5.5V
- Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 5.0MHz @ 3.6V - 5.5V
- Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- 6 wake-up sources
- 7 interrupt sources
- **Universal Asynchronous Receiver and Transmitter (UART)**
- Serial SRAM interface
- BUS memory interface
- Voltage Regulator for external memory devices
- Built-in voltage regulator for external memory devices
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 70 segments, up to 16 commons, maximum 1120 dots**
 - 1/5 bias; 1/16 duty capability (EV chip: 1/5, 1/6 bias; 1/16 duty and 1/32 duty)
 - **140 bytes dedicated LCD RAM**
 - Voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 5.75V, in 1/5 bias)
- Power saving SLEEP mode
- **Low Voltage Detector**
 - **8-level 2.9V - 2.4V/4.35V – 3.3V detection**
 - **2.2V Low voltage reset**
- Peripherals
 - **Max. 29 I/O pins (PA[7:0], PB[7:0], PC[7:0], PD[4:0])**
 - Dedicated I/Os: PA[0:4]
 - Shared pin I/Os:
 - PA[5:7]/SEG[69:67]
 - PB[0:7]/BMI AD BUS[0:7]/SEG[64:57]
 - PC[0:1]/BMI MC[0:1]/SSRAM SDA, SCK
 - PC[2:3]/UART Tx/Rx/SEG[66:65]
 - PC[4:5]/SEG[56:55]/Ext_I , Ext_CK
 - PC[6:7]/SEG[54:53]
 - PD[0:4]/SEG[52:48]
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - **8-bit DAC resolution, 2-ch PWM audio outputs**
 - Watchdog Timer

2.3.2. GPLB31

- Built-in 8-bit processor
- **4288 bytes SRAM**
- **256K bytes ROM**
- Operating voltage: 2.4V - 3.6V, 3.6V - 5.5V
- Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 5.0MHz @ 3.6V - 5.5V
- Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- Provides 6 wake-up sources
- Provides 7 interrupt sources
- **Universal Asynchronous Receiver and Transmitter**
- Serial SRAM interface
- BUS memory interface
- Voltage Regulator for external memory devices
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 74 segments, up to 32 commons, 2368 dots max.**
 - 1/5, 1/6 **bias**; 1/16 duty and 1/32 duty capability (EV chip: 1/5, 1/6 bias; 1/16 duty and 1/32 duty)
 - **296 bytes dedicated LCD RAM**
 - Voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 5.75V, 1/5 bias; 2.95V ~ 6.85V, 1/6 bias)
- Power saving SLEEP mode
- **Low voltage detector**
 - **8-level 2.9V - 2.4V/4.35V - 3.3V detection**
 - **2.2V Low voltage reset**
- Peripherals
 - **Max. 29 I/O pins (PA[7:0], PB[7:0], PC[7:0], PD[4:0])**
 - Dedicated I/Os: PA[2:0]
 - Shared pin I/Os:
 - PA[3:7]/SEG[73:69]
 - PB[7:0]/BMI AD Bus [7:0]
 - PC[1:0]/BMI MC[1:0]/SSRAM SDA, SCK
 - PC[2:3]/UART Tx/Rx
 - PC[4:5]/SEG[68:67]/Ext_I , Ext_CK
 - PC[6:7]/SEG[66:65]
 - PD[0:4]/COM[31:27]
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - **8-bit DAC resolution, 2-ch PWM audio outputs**
 - Watchdog Timer

2.3.3. GPLB32

- Built in 8-bit processor
 - **1216 bytes SRAM**
 - **512K bytes ROM**
 - Wide operating voltage range: 2.4V - 3.6V, 3.6V - 5.5V
 - Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 5.0MHz @ 3.6V - 5.5V
 - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
 - Provides 6 wake-up sources
 - Provides 7 interrupt sources
- Universal Asynchronous Receiver and Transmitter (UART)
- Serial SRAM interface
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **74 segments, 16 commons, maximum 1184 dots or 64 segments, 32 commons, maximum 2048 dots**
 - 1/5, 1/6 bias; 1/16, 1/32 duty capability
 - 296 bytes dedicated LCD RAM
 - Built-in voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 5.75V, 1/5 bias; 2.95V ~ 6.85V, 1/6 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 8-level, 2.9V - 2.4V/4.35V - 3.3V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 28 I/O pins (PA[7:0], PB[5:0], PC[7:0], PD[5:0])**
 - Dedicated I/Os: PA[0:5]
 - Shared pin I/Os:
 - PA[6:7] / SEG[63:62]
 - PB[0:5] / SEG[69:64] / COM[21:16]
 - PC[0:1] / SSRAM SCK, SDA/SEG[61:60]
 - PC[2:3] / UART Tx/Rx
 - PC[4:5] / SEG[73:72] / COM[25:24]/Ext_I, Ext_ck
 - PC[6:7] / SEG[71:70] / COM[23:22]
 - PD[0:5] / COM[31:26]
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - 8-bit DAC resolution, 2-channel PWM/DAC audio outputs
 - Watchdog Timer for reliable operation

2.3.4. GPLB33A

- Built in 8-bit processor
 - **1216 bytes SRAM**
 - **64K bytes ROM**
 - Wide operating voltage range: 2.4V - 3.6V, 3.6V - 5.5V
 - Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 5.0MHz @ 3.6V - 5.5V
 - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
 - Provides 6 wake-up sources
 - Provides 7 interrupt sources
- Serial SRAM interface
- Universal Asynchronous Receiver and Transmitter (UART)
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 52 segments, 16 commons, max 832 dots**
 - 1/5 bias; 1/16 duty capability
 - 104 bytes dedicated LCD RAM
 - Built-in voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 5.75V, in 1/5 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 8-level 2.9V – 2.4V/4.35V - 3.3V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 24 I/O pins (PA[7:0], PB[7:0], PC[7:0])**
 - Dedicated I/Os: PA[0:6]
 - Shared pin I/Os:
 - PA[7] / SEG[51]
 - PB[0:7] / SEG[46:39]
 - PC[0:1] / SSRAM SCK, SDA
 - PC[2:3] / UART Tx/Rx
 - PC[4:5] / SEG[50:49] / Ext_I , Ext_ck
 - PC[6:7] / SEG[48:47]
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - 8-bit DAC resolution, 2-channel PWM audio outputs
 - Watchdog Timer for reliable operation

2.3.5. GPLB33B

- Built in 8-bit processor
 - **1024 bytes SRAM**
 - **96K bytes ROM**
 - Wide operating voltage range: 2.4V - 3.6V,
 - Max. operating speed: 4.0MHz @ 2.4V - 3.6V,
 - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
 - Provides 5 wake-up sources
 - Provides 5 interrupt sources
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 48 segments, 16 commons, max 768 dots**
 - 1/3, 1/4, 1/5 bias; 1/4, 1/8, 1/16 duty capability
 - 96 bytes dedicated LCD RAM
 - Built-in voltage regulator to generate VLCD for LCD driver
 - 27-level contrast control (2.98V ~ 5.75V, in 1/3~1/5 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 6-level 2.9V – 2.4V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 24 I/O pins (PA[7:0], PB[7:0], PC[7:0])**
 - Dedicated I/Os: PA[0:7], PC[0:1]
 - Shared pin I/Os:
 - PB[0:7] / SEG[41:34]
 - PC[2:7] / SEG[47:42]
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - 8-bit DAC resolution, 2-channel PWM audio outputs
 - Watchdog Timer for reliable operation
- Low power consumption
 - 600 μ A typical @ 3.0V, F_{CPU} = 1.0MHz, F_{OSC} = 4.0MHz
 - 30 μ A typical halt current @ 3.0V
 - <1 μ A typical standby current @ 3.0V

2.3.6. GPLB34

- 8-bit micro-processor
- **2752 bytes SRAM**
- **1M bytes ROM**
- Operating voltage: 2.4V - 3.6V, 3.6V - 5.5V
- Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 6.0MHz @ 3.6V - 5.5V
- Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- 6 wake-up sources
- 7 interrupt sources
- **Universal Asynchronous Receiver and Transmitter (UART)**
- Serial SRAM interface
- BUS memory interface
- Voltage Regulator for external memory devices
- Built-in voltage regulator for external memory devices
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 74 segments, up to 32 commons, maximum 2368 dots**
 - 1/5, 1/6 bias; 1/16, 1/32 duty capability
 - **296 bytes dedicated LCD RAM**
 - Voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 5.75V, 1/5 bias; 2.95V ~ 6.85V, 1/6 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 6-level 2.9V - 2.4V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 21 I/O pins (PA[7:0], PB[7:0], PC[4:0])**
 - Dedicated I/Os: PA[0:7]
 - Shared pin I/Os:
 - PB[0:7]/BMI AD BUS[0:7]
 - PC[0:1]/BMI MC[0:1]/SSRAM SCK, SDA,
 - PC[2:3]/UART Tx/Rx
 - PC[4]/External Interrupt
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - **8-bit DAC resolution, 2-ch PWM audio outputs**
 - Watchdog Timer

2.3.7. GPLB35

- 8-bit micro-processor
- **2752 bytes SRAM**
- **1M bytes ROM**
- Operating voltage: 2.4V - 3.6V, 3.6V - 5.5V
- Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 6.0MHz @ 3.6V - 5.5V
- Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- 6 wake-up sources
- 7 interrupt sources
- **Universal Asynchronous Receiver and Transmitter (UART)**
- Serial SRAM interface
- **SPI interface**
- BUS memory interface
- Voltage Regulator for external memory devices
- Built-in voltage regulator for external memory devices
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 100 segments, up to 48 commons, maximum 4032 dots**
 - 1/5, 1/6, 1/7, 1/8 bias; 1/16, 1/32, 1/36, 1/48 duty capability
 - **600 bytes dedicated LCD RAM**
 - Voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 8.21V, 1/5 - 1/8 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 6-level 2.9V - 2.4V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 21 I/O pins (PA[7:0], PB[7:0], PC[4:0])**
 - Dedicated I/Os: PA[0:4]
 - Shared pin I/Os:
 - PA[5:7]/SPI SDO , SDI , SCK,
 - PB[0:7]/BMI AD BUS[0:7]
 - PC[0:1]/BMI MC[0:1]/SSRAM SCK ,SDA,
 - PC[2:3]/UART Tx/Rx
 - PC[4]/External Interrupt
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - **8-bit DAC resolution, 2-ch PWM audio outputs**
 - Watchdog Timer

2.3.8. GPLB36

- 8-bit micro-processor
- **2752 bytes SRAM**
- **512K bytes ROM**
- Operating voltage: 2.4V - 3.6V, 3.6V - 5.5V
- Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 6.0MHz @ 3.6V - 5.5V
- Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- 6 wake-up sources
- 7 interrupt sources
- **Universal Asynchronous Receiver and Transmitter (UART)**
- Serial SRAM interface
- **SPI interface**
- BUS memory interface
- Voltage Regulator for external memory devices
- Built-in voltage regulator for external memory devices
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 100 segments, up to 48 commons, maximum 4032 dots**
 - 1/5, 1/6, 1/7, 1/8 bias; 1/16, 1/32, 1/36, 1/48 duty capability
 - **600 bytes dedicated LCD RAM**
 - Voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 8.21V, 1/5 - 1/8 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 6-level 2.9V - 2.4V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 21 I/O pins (PA[7:0], PB[7:0], PC[4:0])**
 - Dedicated I/Os: PA[0:4]
 - Shared pin I/Os:
 - PA[5:7]/SPI SDO , SDI , SCK,
 - PB[0:7]/BMI AD BUS[0:7]
 - PC[0:1]/BMI MC[0:1]/SSRAM SCK ,SDA,
 - PC[2:3]/UART Tx/Rx
 - PC[4]/External Interrupt
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - **8-bit DAC resolution, 2-ch PWM audio outputs**
 - Watchdog Timer

2.3.9. GPLB37

- Built in 8-bit processor
 - **1216 bytes SRAM**
 - **256K bytes ROM**
 - Wide operating voltage range: 2.4V - 3.6V, 3.6V - 5.5V
 - Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 5.0MHz @ 3.6V - 5.5V
 - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
 - Provides 6 wake-up sources
 - Provides 7 interrupt sources
- Universal Asynchronous Receiver and Transmitter (UART)
- Serial SRAM interface
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **74 segments, 16 commons, maximum 1184 dots or 64 segments, 32 commons, maximum 2048 dots**
 - 1/5, 1/6 bias; 1/16, 1/32 duty capability
 - 296 bytes dedicated LCD RAM
 - Built-in voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 5.75V, 1/5 bias; 2.95V ~ 6.85V, 1/6 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 8-level 2.9V - 2.4V/4.35V - 3.3V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 28 I/O pins (PA[7:0], PB[5:0], PC[7:0], PD[5:0])**
 - Dedicated I/Os: PA[0:5]
 - Shared pin I/Os:
 - PA[6:7] / SEG[63:62]
 - PC[0:1] / SSRAM SCK, SDA/SEG[61:60]
 - PC[2:3] / UART Tx/Rx
 - PC[4:5] / SEG[73:72] / COM[25:24]/Ext_I, Ext_ck
 - PC[6:7] / SEG[71:70] / COM[23:22]
 - PB[0:5] / SEG[69:64] / COM[21:16]
 - PD[0:5] / COM[31:26]
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters
 - 8-bit DAC resolution, 2-channel PWM/DAC audio outputs
 - Watchdog Timer for reliable operation

2.3.10. GPLB39

- 8-bit micro-processor
- **8128 bytes SRAM**
- **2M bytes ROM**
- Operating voltage: 2.4V - 3.6V, 3.6V - 5.5V
- Max. operating speed: 4.0MHz @ 2.4V - 3.6V, 6.0MHz @ 3.6V - 5.5V
- Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- 6 wake-up sources
- 7 interrupt sources
- **Universal Asynchronous Receiver and Transmitter (UART)**
- Serial SRAM interface
- SPI interface
- BUS memory interface
- Voltage Regulator for external memory devices
- Built-in voltage regulator for external memory devices
- Key scan function
 - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
 - **Up to 112 segments, up to 64 commons, maximum 6144 dots**
 - 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 bias; 1/8, 1/16, 1/32, 1/36, 1/48, 1/64 duty capability
 - **896 bytes dedicated LCD RAM**
 - Voltage regulator to generate VLCD for LCD driver
 - 32-level contrast control (2.45V ~ 8.05V, 1/4 - 1/8 bias)
- Power saving SLEEP mode
- Low Voltage Detector
 - 8-level 2.9V - 2.4V/4.35V - 3.3V detection
 - 2.2V Low voltage reset
- Peripherals
 - **Max. 21 I/O pins (PA[7:0], PB[7:0], PC[4:0])**
 - Dedicated I/Os: PA[0:4]
 - Shared pin I/Os:
 - PA[5:7]/SPI SDO, SCK, SDI,
 - PB[0:7]/BMI AD BUS[0:7]
 - PC[0:1]/BMI MC[0:1]/SSRAM SCK, SDA,
 - PC[2:3]/UART Tx/Rx
 - PC[4]/External Interrupt
 - 32.768KHz oscillator circuit for RTC
 - RC-oscillator (only one resistor is needed)
 - Two 16-bit re-loadable timer/counters/
 - **8-bit DAC resolution, 2-ch PWM audio outputs**
 - Watchdog Timer

3. Memory Mapping

3.1. ROM

- * **GPLB30:** 96K-byte, \$00000 ~ \$17FFF, 3 banks
- * **GPLB31:** 256K-byte, \$00000 ~ \$3FFFF, 8 banks
- * **GPLB32:** 512K-byte, \$00000 ~ \$7FFFF, 16 banks
- * **GPLB33A:** 64K-byte, \$00000 ~ \$0FFFF, 2 banks
- * **GPLB33B:** 96K-byte, \$00000 ~ \$17FFF, 3 banks
- * **GPLB34:** 1M-byte, \$00000 ~ \$FFFFFF, 32 banks
- * **GPLB35:** 1M-byte, \$00000 ~ \$FFFFFF, 32 banks
- * **GPLB36:** 512K-byte, \$00000 ~ \$7FFFF, 16 banks
- * **GPLB37:** 256K-byte, \$00000 ~ \$3FFFF, 8 banks
- * **GPLB39:** 2M-byte, \$00000 ~ \$1FFFFFF, 64banks
- * **LB30EV Chip:** Up to 1M-byte
- * **LB35EV Chip:** Up to 2M-byte
- * **LB39EV Chip:** Up to 2M-byte

3.2. RAM

- * **GPLB30:** 2752-byte, \$40 ~ \$AFF
- * **GPLB31:** 4288-byte, \$40 ~ \$10FF
- * **GPLB32:** 1216-byte, \$40 ~ \$4FF
- * **GPLB33A:** 1216-byte, \$40 ~ \$4FF
- * **GPLB33B:** 1024-byte, \$40 ~ \$43F
- * **GPLB34:** 2752-byte, \$40 ~ \$AFF
- * **GPLB35:** 2752-byte, \$40 ~ \$AFF
- * **GPLB36:** 2752-byte, \$40 ~ \$AFF
- * **GPLB37:** 1216-byte, \$40 ~ \$4FF
- * **GPLB39:** 8128-byte, \$40 ~ \$1FFF
- * **LB30EV Chip:** 8128-byte, \$40 ~ \$1FFF
- * **LB35EV Chip:** 2816-byte, \$40 ~ \$1FFF
- * **LB39EV Chip:** 8128-byte, \$40 ~ \$1FFF

3.3. Memory Mapping Diagram

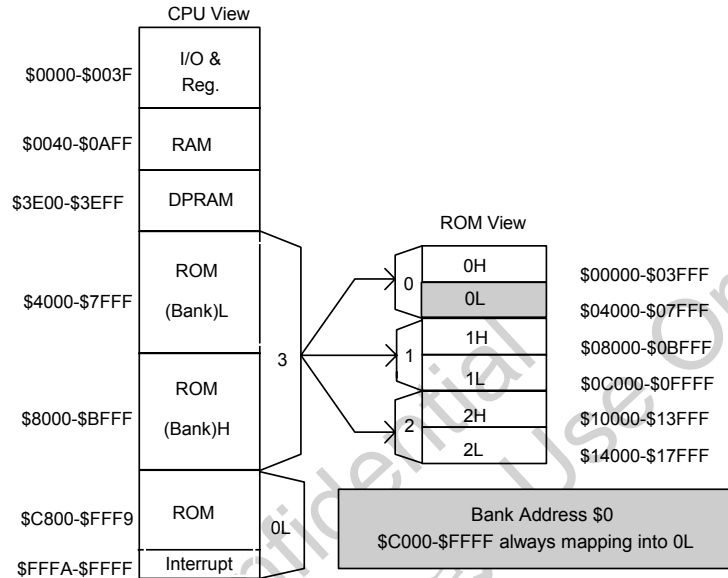
GPLB30

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH(128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0B00-\$3DFF is reserved.

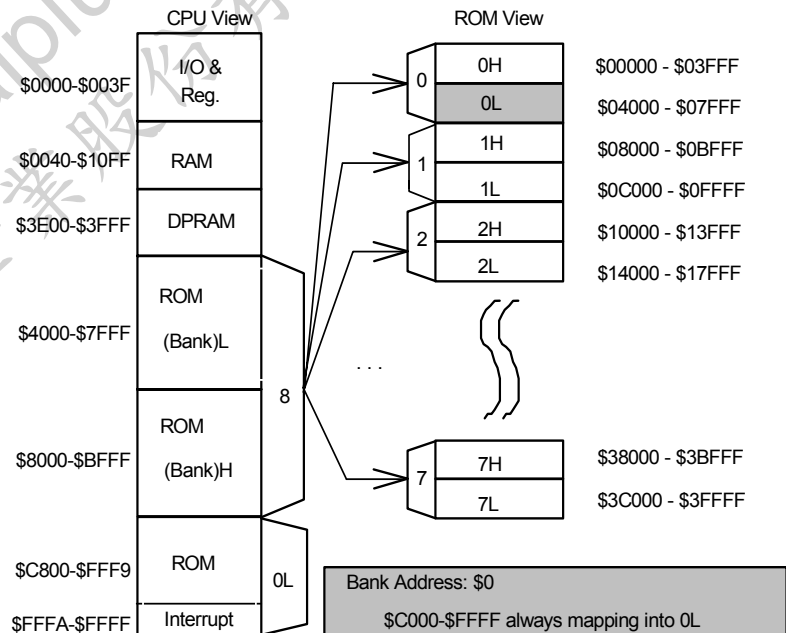
GPLB31

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH(128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$1100-\$3DFF is reserved.

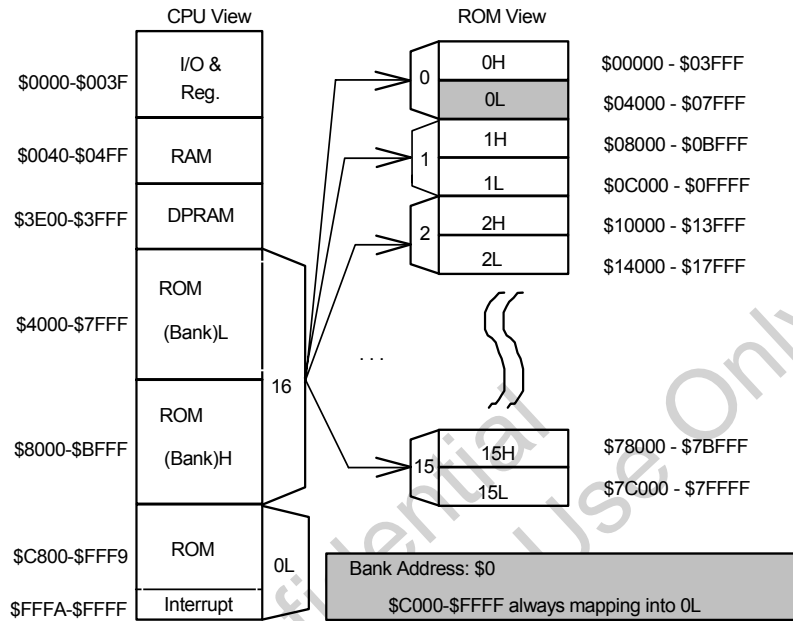
GPLB32

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0500-\$3DFF is reserved.

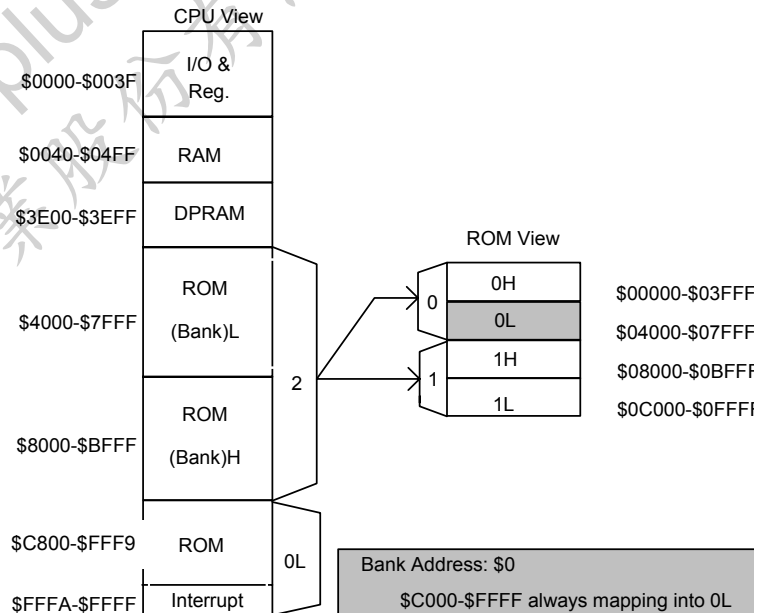
GPLB33A

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0500-\$3DFF is reserved.

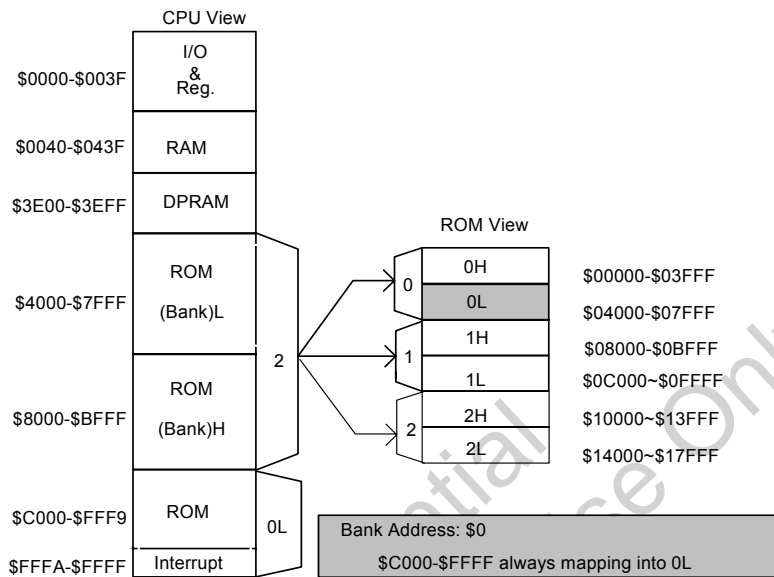
GPLB33B

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1



\$0440-\$3DFF is reserved.

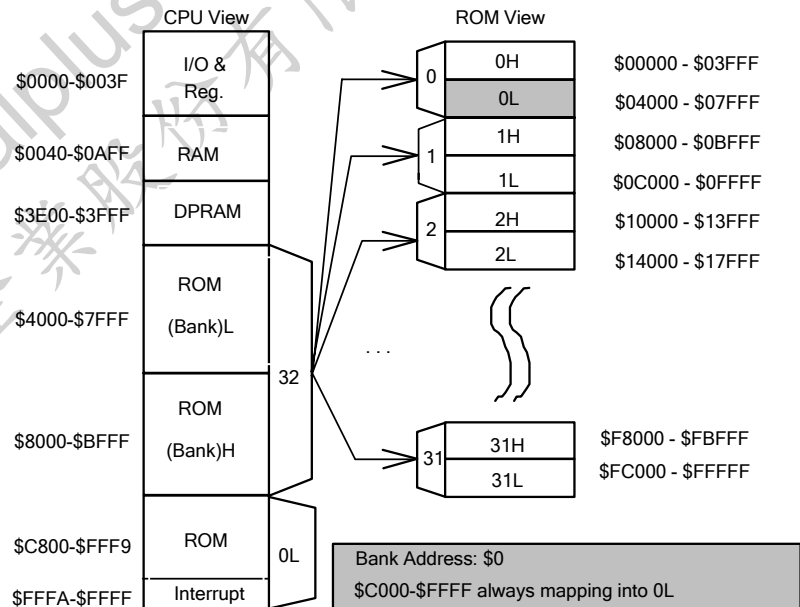
GPLB34

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH(128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0B00-\$3DFF is reserved.

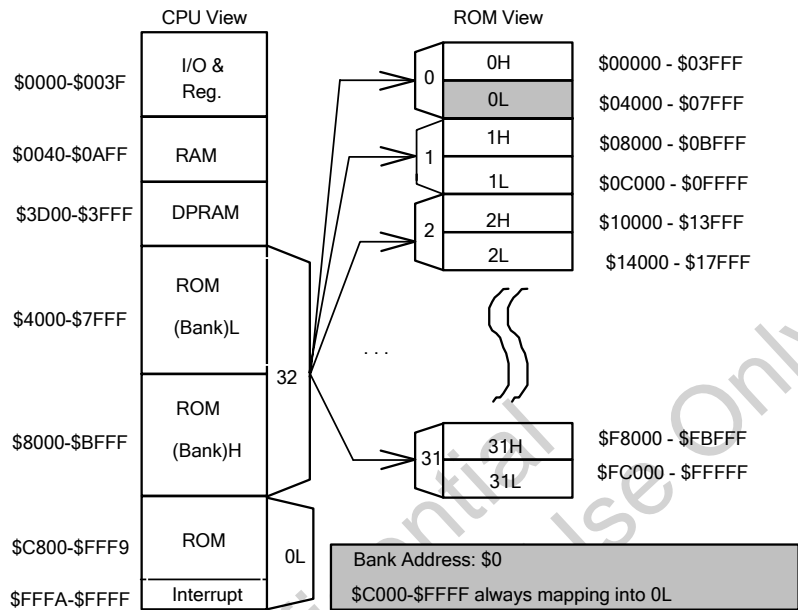
GPLB35

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH(128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0B00-\$3CFF is reserved.

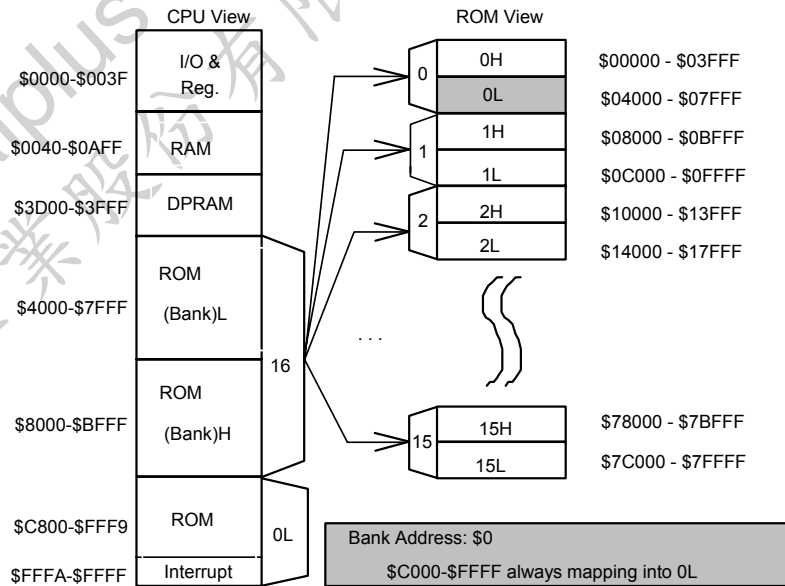
GPLB36

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0B00-\$3CFF is reserved.

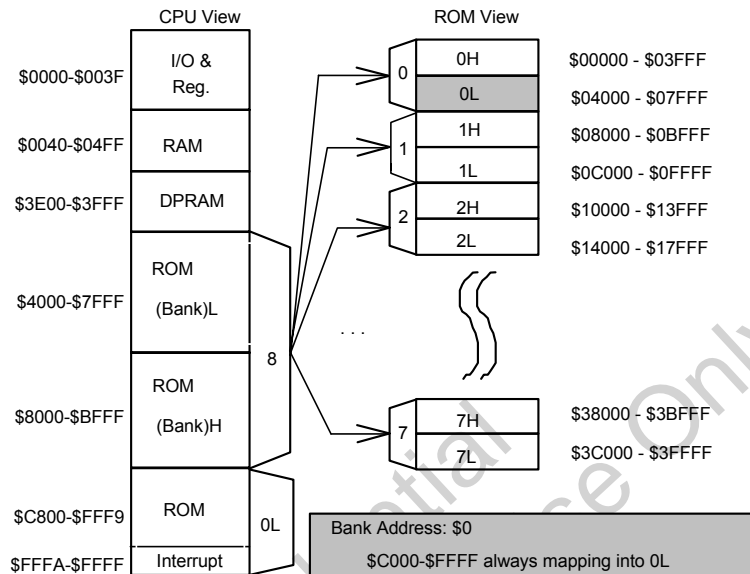
GPLB37

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH(128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$0500-\$3DFF is reserved.

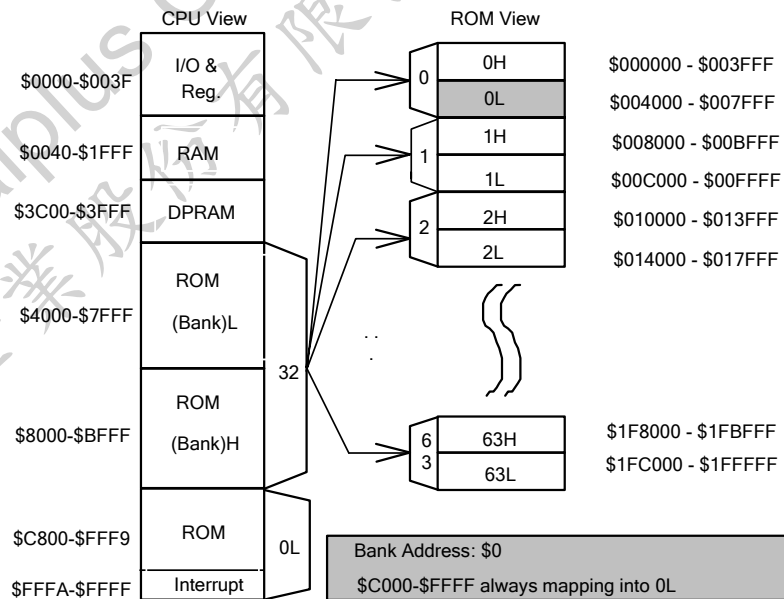
GPLB39

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH(128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



\$2000-\$3BFF is reserved.

Note:

1. \$4000-\$BFFF can be external memory if MEXT (\$03.7) = 1 and Bank port (\$00.7) = 1.
2. \$C000-\$FFFF can be external memory if MEXT (\$03.7) = 1 and EXC (\$0b.1) = 1.
3. User program should start from \$C800. \$C000-\$C7FF is the test program area.
4. User program interrupt vector: \$FFFA ~ \$FFFF
5. Test program interrupt vector: \$FFF2 ~ \$FFF7

3.4. RAM Size Selection

The RAM size on GPLB30EV-chip can be selected by SRAMSZ1 and SRAMSZ0.

(SRAMSZ1, SRAMSZ0)	Data SRAM Size	Address Range
(0,0)	1KB+192	\$40-4FF
(0,1)	2.5KB+192	\$40-AFF
(1,0)	4KB+192	\$40-10FF
(1,1)	8128 Byte	\$40-1FFF

3.5. DPRAM Size Selection on GPLB30EV

DPRAMSZ	DPRAM Size	Address Range
0	74 x 16-bit	\$3E00-3EFF
1	74 x 32-bit	\$3E00-3FFF

3.6. P_00H_Bank_Sel (\$00) (R/W) (Default: 00000000)

The P_00H_Bank_Sel configures bank selections. Write a value to this port to switch between banks.

P_Bank_Sel		0x00		Bank Selection					
Bit	7	6	5	4	3	2	1	0	
Function	Ext SEL	-	Bank SEL						
Default	0	0	0	0	0	0	1	0	

Bit	Function	Type	Description	Condition
7	Ext SEL	W	When external memory is accessed, \$00.7 & 03.7 must be set to "1" mapping address = 4000H- BFFFH	
		R	Read this bit status	
5:0	Bank SEL	W	Memory bank selection	See below table
		R	Read current bank status	

b5	b4	b3	b2	b1	b0	Bank	Address Range
0	0	0	0	0	0	Bank0	\$00000 - \$07FFF
0	0	0	0	0	1	Bank1	\$08000 - \$0FFFF
0	0	0	0	1	0	Bank2	\$10000 - \$17FFF
0	0	0	0	1	1	Bank3	\$18000 - \$1FFFF
0	0	0	1	0	0	Bank4	\$20000 - \$27FFF
0	0	0	1	0	1	Bank5	\$28000 - \$2FFFF
0	0	0	1	1	0	Bank6	\$30000 - \$37FFF
0	0	0	1	1	1	Bank7	\$38000 - \$3FFFF
0	0	1	0	0	0	Bank8	\$40000 - \$47FFF
0	0	1	0	0	1	Bank9	\$48000 - \$4FFFF
0	0	1	0	1	0	Bank10	\$50000 - \$57FFF
0	0	1	0	1	1	Bank11	\$58000 - \$5FFFF
0	0	1	1	0	0	Bank12	\$60000 - \$67FFF

b5	b4	b3	b2	b1	b0		
0	0	1	1	0	1	Bank13	\$68000 - \$6FFFF
0	0	1	1	1	0	Bank14	\$70000 - \$77FFF
0	0	1	1	1	1	Bank15	\$78000 - \$7FFFF
0	1	0	0	0	0	Bank16	\$80000 - \$87FFF
0	1	0	0	0	1	Bank17	\$88000 - \$8FFFF
0	1	0	0	1	0	Bank18	\$90000 - \$97FFF
0	1	0	0	1	1	Bank19	\$98000 - \$9FFFF
0	1	0	1	0	0	Bank20	\$A0000 - \$A7FFF
0	1	0	1	0	1	Bank21	\$A8000 - \$AFFFF
0	1	0	1	1	0	Bank22	\$B0000 - \$B7FFF
0	1	0	1	1	1	Bank23	\$B8000 - \$BFFFF
0	1	1	0	0	0	Bank24	\$C0000 - \$C7FFF
0	1	1	0	0	1	Bank25	\$C8000 - \$CFFFF
0	1	1	0	1	0	Bank26	\$D0000 - \$D7FFF
0	1	1	0	1	1	Bank27	\$D8000 - \$DFFFF
0	1	1	1	0	0	Bank28	\$E0000 - \$E7FFF
0	1	1	1	0	1	Bank29	\$E8000 - \$EFFFF
0	1	1	1	1	0	Bank30	\$F0000 - \$F7FFF
0	1	1	1	1	1	Bank31	\$F8000 - \$FFFFF
1	0	0	0	0	0	Bank32	\$100000 - \$107FFF
1	0	0	0	0	1	Bank33	\$108000 - \$10FFFF
1	0	0	0	1	0	Bank34	\$110000 - \$117FFF
1	0	0	0	1	1	Bank35	\$118000 - \$11FFFF
1	0	0	1	0	0	Bank36	\$120000 - \$127FFF
1	0	0	1	0	1	Bank37	\$128000 - \$12FFFF
1	0	0	1	1	0	Bank38	\$130000 - \$137FFF
1	0	0	1	1	1	Bank39	\$138000 - \$13FFFF
1	0	1	0	0	0	Bank40	\$140000 - \$147FFF
1	0	1	0	0	1	Bank41	\$148000 - \$14FFFF
1	0	1	0	1	0	Bank42	\$150000 - \$157FFF
1	0	1	0	1	1	Bank43	\$158000 - \$15FFFF
1	0	1	1	0	0	Bank44	\$160000 - \$167FFF
1	0	1	1	0	1	Bank45	\$168000 - \$16FFFF
1	0	1	1	1	0	Bank46	\$170000 - \$177FFF
1	0	1	1	1	1	Bank47	\$178000 - \$17FFFF
1	1	0	0	0	0	Bank48	\$180000 - \$187FFF
1	1	0	0	0	1	Bank49	\$188000 - \$18FFFF
1	1	0	0	1	0	Bank50	\$190000 - \$197FFF
1	1	0	0	1	1	Bank51	\$198000 - \$19FFFF
1	1	0	1	0	0	Bank52	\$1A0000 - \$1A7FFF
1	1	0	1	0	1	Bank53	\$1A8000 - \$1AFFFF
1	1	0	1	1	0	Bank54	\$1B0000 - \$1B7FFF
1	1	0	1	1	1	Bank55	\$1B8000 - \$1BFFFF
1	1	1	0	0	0	Bank56	\$1C0000 - \$1C7FFF
1	1	1	0	0	1	Bank57	\$1C8000 - \$1CFFFF
1	1	1	0	1	0	Bank58	\$1D0000 - \$1D7FFF
1	1	1	0	1	1	Bank59	\$1D8000 - \$1DFFFF
1	1	1	1	0	0	Bank60	\$1E0000 - \$1E7FFF
1	1	1	1	0	1	Bank61	\$1E8000 - \$1EFFFF
1	1	1	1	1	0	Bank62	\$1F0000 - \$1F7FFF
1	1	1	1	1	1	Bank63	\$1F8000 - \$1FFFFF

4. Operation Modes

There are three operation modes involved in GPLB3X: standby, halt, and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver...) are activated. Generally speaking, this mode consumes the highest power.

Standby Mode

Write "07H" to P_04H_CPU_Clk_Ctrl Register (\$04) and make \$0E.7=0(C32KEN) to activate standby mode. The standby mode is a mode where the device is placed in its lowest power consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

Halt Mode

Write "07H" to P_04H_CPU_Clk_Ctrl Register (\$04) and make \$0E.7=1(C32KEN) to enter halt mode, but still keeps 32768Hz oscillator running. In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

Wake-up Source

The device can be awakened from standby and halt modes via one of the following events:

1. KeyEN PortA key wake-up
2. TBLEN 2Hz, 4Hz, 8Hz, 16Hz wake up
3. TM0EN Timer0 overflow wake-up
4. TBHEN 128Hz, 256Hz, 512Hz, 1KHz wake-up
5. TM1EN Timer1 overflow wake-up
6. RxEN UART Rx signal wake-up

Refer to Register \$18 for more information about how to enable and disable these wake-up sources. If a wake-up event occurs, the next instruction at the moment of entering sleep will be executed.

5. Clock

5.1. CPU Clock

CPU clock can be controlled by P_04H_CPU_Clk_Ctrl (\$04). The default and initial (after reset and wake-up) clock is $F_{osc}/4$ (b2=0, b1=1, b0=0) where F_{osc} is the frequency from R-oscillator.

5.1.1. P_04H_CPU_Clk_Ctrl (\$04)(Default: 00000010)

P_CPU_Clk_Ctrl		0x04			CPU Clock Control			
Bit	7	6	5	4	3	2	1	0
Function	PWM CK SEL	-	-	-	-	CKS2	CKS1	CKS0
Default	0	0	0	0	0	0	1	0

Bit	Function	Type	Description	Condition
7	PWM CK SEL	W	PWM clock selection	0 = F_{osc} 1 = $F_{osc}/2$
[2:0]	CKS	W	CPU clock select	000 = F_{osc} 001 = $F_{osc}/2$ 010 = $F_{osc}/4$ (Default) 011 = $F_{osc}/8$ 100 = $F_{osc}/16$ 101 = $F_{osc}/32$ 110 = $F_{osc}/64$ 111 = Sleep, CPU stops

5.1.2. P_0EH_32768_EN (\$0E) (W)

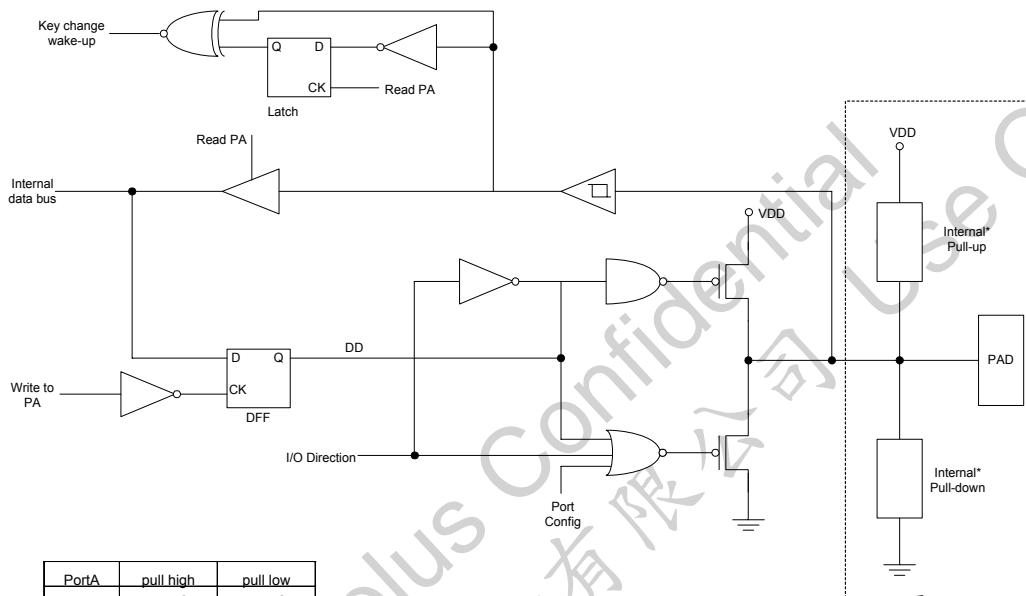
P_CPU_Clk_Ctrl		0x0E			32768Hz OSC. Enable			
Bit	7	6	5	4	3	2	1	0
Function	C32KEN	-	-	-	-	-	-	-
Default	1	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	C32KEN	W	All LCD driver, voltage detector, regulator, watchdog, and low voltage reset functions are valid only when 32768Hz oscillator is enabled	0 = Disable 32768 clock 1 = Enable 32768 clock

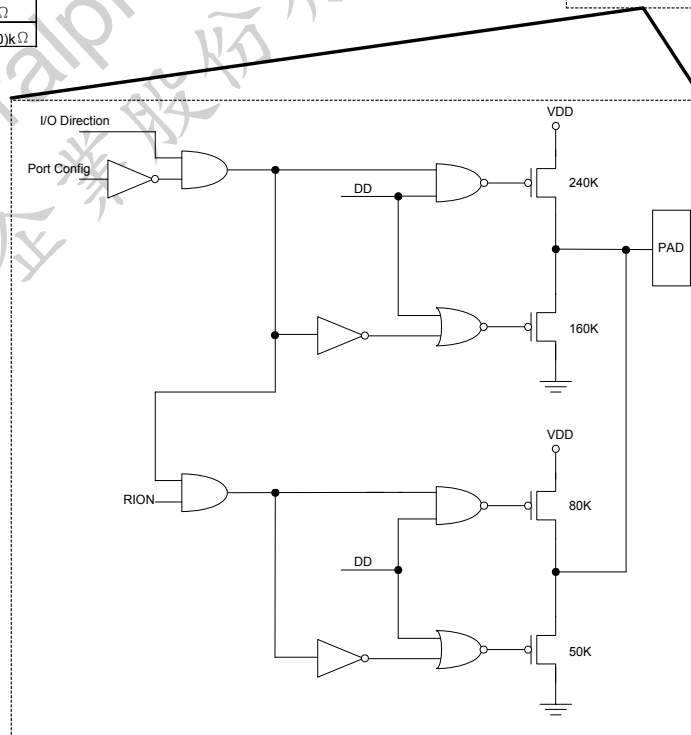
6. I/O Configuration

6.1. I/O Structure

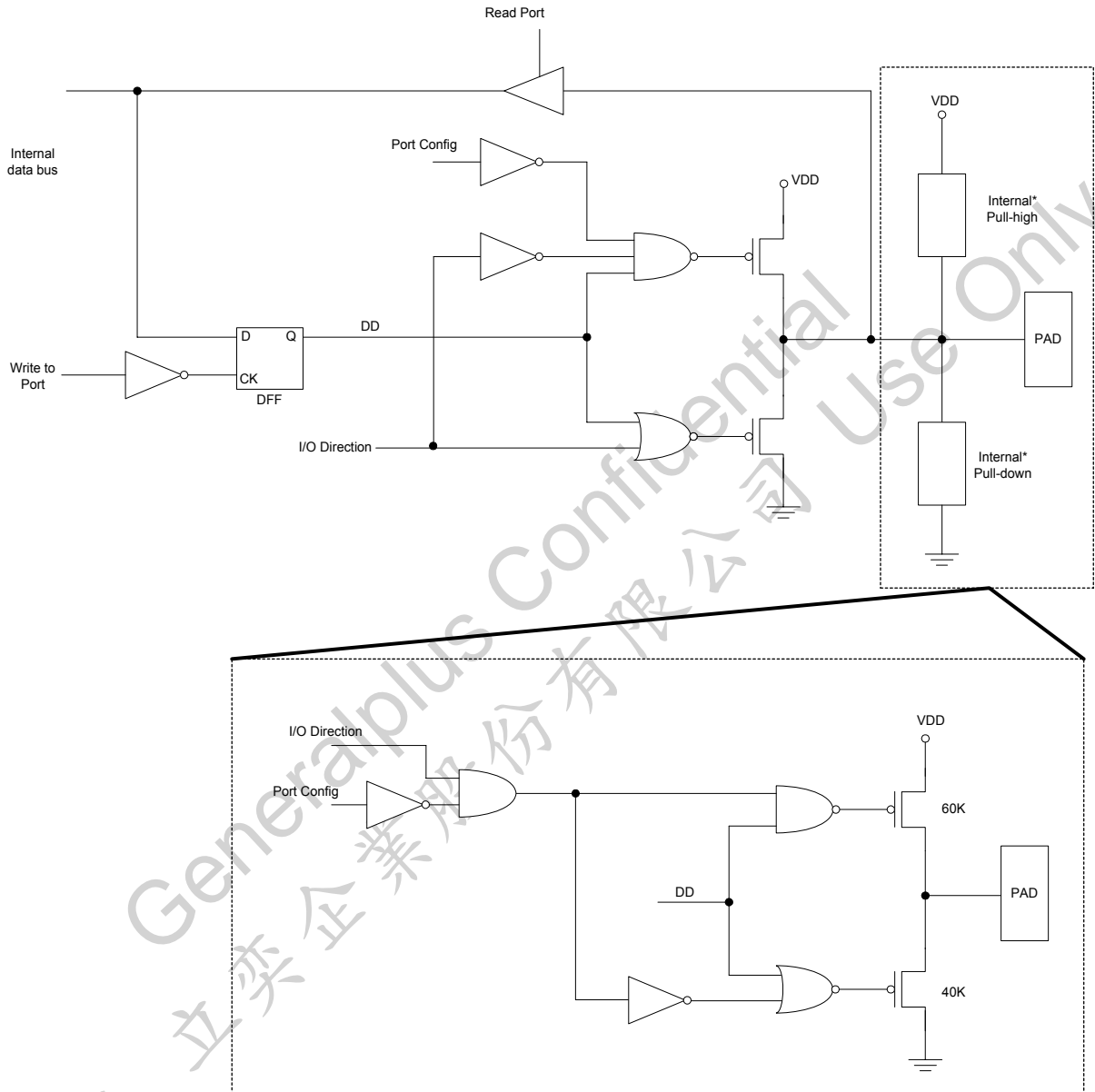
6.1.1. PortA



PortA	pull high	pull low
weak	240k Ω	160k Ω
strong	(240 80)k Ω	(160 50)k Ω



6.1.2. Port B, C, D



- *I/O capability Input and Output. Default: input with pull-low resistor
- *Input type Pull-high, Pull-low, Pure
- *Output type CMOS buffer, ODP (Open Drain PMOS), ODN (Open Drain NMOS)

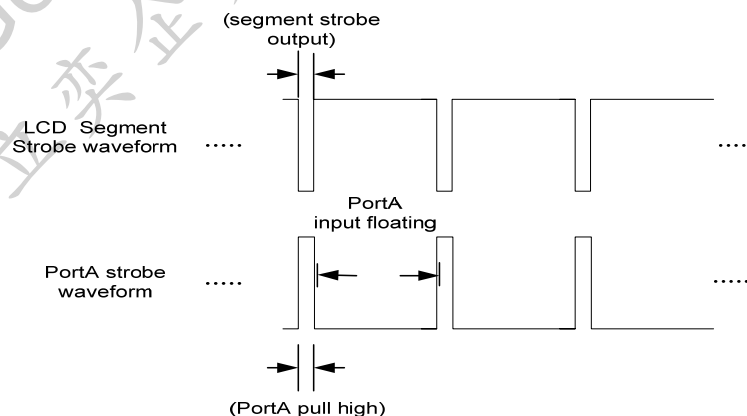
6.2. P_05H_Port A_Strobe_Pull (\$05) (R/W)

P_PortA_Strobe_pull		0x05			PortA Strobe Enable			
Bit	7	6	5	4	3	2	1	0
Function	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	STRB	W	PortA either normal I/O or synchronized with LCD stobe waveform. Note: 1. If Port A strobe function enable , PortA must be set input. 2. PortA is floating most of time except it is pull low/high during the LCD strobe interval (see the diagram below).	0:Port A is normal I/O 1:Port A strobe function enable (synchronized with LCD strobe waveform)
		R	Read this bit status	

Note:

1. **If hardware key scan is used**, to avoid influencing LCD display while pressing keys, PortA strobe should remain enabled unless PortA is being read and need to disable strobe function to get the correct data (always pull high/low).
2. **The data can only be read within the strobe interval if strobe is enabled (see the following diagram).** Therefore, to ensure data is read correctly and thoroughly, Port A strobe must be disabled. In other words, the data can be read from PortA anytime if PortA strobe is disabled.
3. Besides the strobe interval, PortA status is input floating but it will always be read as logic high.



Example:

initialization:

```

lda #0ffh ; enable $05 all the time as program is running
sta P_05H_Port A_Strobe_Pull ;
.....

```

```

KeyScan:                                     ; disable $05 only as reading key
;put keyscan data in $3B and $3C first
lda #0
sta P_05H_Port A_Strobe_Pull ; disable PortA strobe function and change to normal input
tax
lda #0x00000000
sta P_24H_LCD_Option_Setting ; disable LCD strobe waveform
lda #0x10000011
sta P_3AH_Keyscan_Ctrl ; strong pull-high/seg key scan output enable
%Dealy_1us ; Delay about 1us to ensure Segment[0:15] status is ready
lda P_08H_Port A_Data ; read PortA
stx P_3AH_Keyscan_Ctrl
lda #0ffh ;
sta P_05H_Port A_Strobe_Pull ; enable $05 after reading key
;
;
;
;
lda #0x00000011
sta P_24H_LCD_Option_Setting ; Enable LCD strobe waveform when exiting the key scan routine

```

6.3. PortA I/Os Function Table

Direction Register(\$07)	Attribution Register(\$06)	Data Register(\$08)	Function	Wakeup	Description
0	0	0	Pull	Yes	Input with pull low
0	0	1	Pull	Yes	Input with pull high
0	1	0	Pure	Yes	Float (High Impedence)
0	1	1	Pure	Yes	Float (High Impedence)
1	0	0	Buffer	No	Output low
1	0	1	Buffer	No	Output high
1	1	0	ODP	No	Float
1	1	1	ODP	No	Output high

6.4. P_07H_Port A_Dir (\$07) (W) (Default: 00H)

P_PortA_Dir	0x07			PortA Direction Register				
Bit	7	6	5	4	3	2	1	0
Function	DIRA7	DIRA6	DIRA5	DIRA4	DIRA3	DIRA2	DIRA1	DIRA0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	PortA Dir	W	It configures PortA input or output setup. When you turn on SPI function ,you can't set this register. H/W will auto-set PA5-7 direction.	Refer to PortA I/Os Function Table
		R	Read this port status	

6.5. P_06H_Port A_Config (\$06)(W)

P_PortA_Config	0x06			PortA Attribution Register				
Bit	7	6	5	4	3	2	1	0
Function	PortA Config							
Default	0	0	0	0	0	0	0	0

6.6. P_08H_Port A_Data/WakeUp (\$08) (R/W)

P_PortA_Data	0x08			PortA Data & Wakeup Port				
Bit	7	6	5	4	3	2	1	0
Function	PortA data							
Default	X	X	X	X	X	X	X	X

X: Unknow

Latch PortA before entering into sleep mode.

Example:

```

lda    #0                                ;
sta    P_05H_Port A_Strobe_Pull        ; disable PortA strobe before read PortA data
%WaitPortAReady                        ; at least 8 CPU clock cycle delay to ensure PortA status is ready
lda    P_08H_Port A_Data                ; latch PortA
lda    #7                                ;
sta    P_04H_CPU_Clk_Ctrl              ; enter sleep mode
nop
nop
  
```

6.7. PortB I/Os Function Table

Direction Register(\$29)	Attribution Register(\$28)	Data Register(\$0A)	Function	Description
0	0	0	Pull	Input with pull low
0	0	1	Pull	Input with pull high
0	1	0	Pure	Float (High Impedence)
0	1	1	Pure	Float (High Impedence)
1	0	0	Buffer	Output low
1	0	1	Buffer	Output high
1	1	0	ODN	Output low
1	1	1	ODN	Float

6.8. P_29H_Port B_Dir (\$29) (W) (Default: 00H)

The P_29H_PortB_Dir configures PortB input or output setup. Write "1" to the corresponding bit for output and "0" for input. DIRB01 represents PortB bit0 and bit1; DIRB23 means PortB bit2 and bit3..., etc. When you turn on BUS extender(MEXT =1 , \$03.7=1), H/W will auto-set PB in/out direction.

P_PortB_Dir		0x29			PortB Direction Register			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	DIRB67	DIRB45	DIRB32	DIRB10
Default	0	0	0	0	0	0	0	0

6.9. P_28H_Port B_Config (\$28) (W) (Default:00H)

The P_28H_PortB_Config sets the attribution of PortB. The attribution depends on the input or output mode.

P_PortB_Config		0x28			PortB Attribution Register			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	PB67	PB45	PB23	PB01
Default	0	0	0	0	0	0	0	0

6.10. P_0AH_Port B_Data/BEXAD_bus (\$0A) (R/W)

If voltage regulator is optioned, the logical high level at PortB is varied according to voltage regulator.

P_PortB_Data		0x0A			PortB data & Bus Extend Data Port			
Bit	7	6	5	4	3	2	1	0
Function	PortB data							
Default	X	X	X	X	X	X	X	X

X: Unknow

6.11. PortC I/Os Function Table

Direction Register(\$2B)	Attribution Register(\$2A)	Data Register(\$0B)	I/O Type Register(\$27)	Function	Description
0	0	0	b3~b0=0	Pull	Input with pull low
0	0	1		Pull	Input with pull high
0	1	0		Pure	Float (High Impedence)
0	1	1		Pure	Float (High Impedence)
1	0	0		Buffer	Output low
1	0	1		Buffer	Output high
1	1	0		ODN	Output low
1	1	1		ODN	Float
X	X	X		b3=1 b2=1	UART
			b1,b0=01	Bus Memory Interface	PC1 as MC1 PC0 as MC0
			b1,b0=1x	Serial SRAM Interface	PC1 as SDA PC0 as SCK

Note:

When function is set to UART, BMI, or SSI (Serial SRAM Interface), \$2B is set, but \$2A & \$0B must be set to pull high/low or pure at input mode.

6.12. P_2BH_Port C_Dir (\$2B)(R/W)

The P_2BH_PortC_Dir configures PortC input or output setup. Write “1” to the corresponding bit for output and “0” for input.

P_Portc_Dir		0x2B			PortC Direction Register			
Bit	7	6	5	4	3	2	1	0
Function	DIRC7	DIRC6	DIRC5	DIRC4	DIRC3	DIRC2	DIRC1	DIRC0
Default	0	0	0	0	0	0	0	0

6.13. P_2AH_Port C_Config (\$2A)(W) (Default: 00H)

The P_2AH_PortC_Config sets the attribution of PortC. The attribution depends on whether the individual pin is input mode or output mode. The following table shows the summary of the PortC attribution in input and output mode.

P_PortC_Config		0x2A			PortC Attribution Register			
Bit	7	6	5	4	3	2	1	0
Function	PortC Config							
Default	0	0	0	0	0	0	0	0

6.14. P_0BH_Port C_Data (\$0B) (R/W) (Default: 00H)

P_PortC_Data		0x0B			PortC Data & Bus Extend Data Port			
Bit	7	6	5	4	3	2	1	0
Function	PC7	PC6	PC5/ECLK	PC4/EXTI	PC3/Rx	PC2/Tx	PC1/MC1/SDA	PC0/MC0/SCK
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	PC7,PC6	R/W	PC[6:7] as I/O	Refer to PortC I/Os Function Table
5	PC5/ECLK	R/W	PC5 as I/O or external clock of Timer0 clock source	
4	PC4/EXTI	R/W	PC4 as I/O or external interrupt (falling edge active)	
3:2	PC3/Rx,PC2/Tx	R/W	PC3 as I/O or UART input,PC2 as I/O or UART output	
1:0	PC1/MC1/SDA PC0/MC0/SCK	R/W	1. PC1 ,PC0 as I/O 2. Bus interface control bit MC1,MC0 3. Serial SRAM interface SDA,SCK	

If voltage regulator is optioned, the logical high level PortC[1:0] is varied according to voltage regulator.

6.15. PortD I/Os Function Table

Direction Register(\$2D)	Attribution Register(\$2C)	Data Register(\$09)	I/O Type Register(\$27)	Function	Description
0	0	0	b5~b4=0	Pull	Input with pull low
0	0	1		Pull	Input with pull high
0	1	0		Pure	Float (High Impedence)
0	1	1		Pure	Float (High Impedence)
1	0	0		Buffer	Output low
1	0	1		Buffer	Output high
1	1	0		ODN	Output low
1	1	1		ODN	Float

6.16. P_2DH_Port D_Dir (\$2D) (W) (Default: 00H)

The P_2DH_PortD_Dir configures PortD input or output setup. Write "1" to the corresponding bit for output and "0" for input. DIRD0 represents PortD bit0; DIRB1 means PortD bit1..., etc.

P_Portd_Dir	0x2D		PortD Direction Register					
Bit	7	6	5	4	3	2	1	0
Function	-	-	DIRD5	DIRD4	DIRD3	DIRD2	DIRD1	DIRD0
Default	0	0	0	0	0	0	0	0

6.17. P_2CH_Port D_Config (\$2C) (W) (Default: 00H)

The P_2CH_PortD_Config sets the attribution of PortD. The attribution depends on whether the individual pin is input mode or output mode. The following table shows the summary of the PortD attribution in input and output mode.

P_PortD_Config	0x2C		PortD Attribution Register					
Bit	7	6	5	4	3	2	1	0
Function	-	-	PD5-Attr	PD4-Attr	PD3-Attr	PD2-Attr	PD1-Attr	PD0-Attr
Default	0	0	0	0	0	0	0	0

6.18. P_09H_Port D_Data (\$09) (R/W) (Default: 00H)

P_PortD_Data	0x09		PortD Data					
Bit	7	6	5	4	3	2	1	0
Function	-	-	PD5	PD4	PD3	PD2	PD1	PD0
Default	0	0	0	0	0	0	0	0

6.19. P_27H_Port CD_Config (\$27) (W) (Default: 00H)

The P_27H_PortCD_Config sets the I/O type of PortC. Some pins in PortC have other special functions rather than ordinary I/O. The PC.2 and PC.3 can be used for UART Tx (UART Transmitting pin) and UART Rx (UART Receiving pin). The PortC.0 and PortC.1 also features serial SRAM interface or bus extender function.

P_PortCD_Config		0x27			PortCD Config Data			
Bit	7	6	5	4	3	2	1	0
Function	-	-	PD1SEL	PD0SEL	PC3SEL	PC2SEL	PC1SEL	PC0SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
5	PD1SEL	W	1: reserved; 0: PD1 as I/O	Refer to PortC I/Os Function Table
4	PD0SEL	W	1: reserved; 0: PD0 as I/O	
3	PC3SEL	W	1: PC3 as UART Rx; 0: PC3 as I/O; If Rx applied, I/O mode is input with the attribution defined in \$2A	
2	PC2SEL	W	1: PC2 as UART Tx; 0: PC2 as I/O; If Tx applied, I/O mode is output with the attribution defined in \$2A	
1:0	PC10S1:PC10S0	W	select PC[1:0] as Serial SRAM interface, Bus Extender or I/O 00: I/O 01:Bus interface control bit MC1, MC0 (used when Bus Extender or Bus Flash applied) 1x: Serial SRAM interface SDA, SCK	

6.20. I/O Program Example

```

;=====
; I/O Configuration
; Suppose the following I/O attributions are expected:
;=====

```

1.

```

PortA.0,1  as pure input
PortA.2    as input pull high
PortA.3    as input pull low
PortA.4    as output high
PortA.5    as output low
PortA.6    as output(ODP)
PortA.7    as output(floating)

```

```

LDA    #%11110000    ;PortA input/output setting
STA    P_07H_ProtADir
LDA    #%11000011    ;PortA configuration setting
STA    P_06H_PortAConfig
LDA    #%010101xx    ;PortA data setting
STA    P_08H_PortAData

```

2.

```

PortB.0,1  as pure input
PortB.2    as input pull high
PortB.3    as input pull low
PortB.4    as output high
PortB.5    as output low
PortB.6    as output(ODN)
PortB.7    as output(floating)

```

```

LDA    #%xxxx1100    ;PortB input/output setting
STA    P_29H_ProtBDir
LDA    #%xxxx1001    ;PortB configuration setting
STA    P_28H_PortBConfig
LDA    #%100101xx    ;PortB data setting
STA    P_0AH_PortBData

```

Note:

1. If PortA.x ODP configuration is selected, the corresponding data bit of \$08 should be set as "1". As a result, it outputs high. It will be configured as floating state if the corresponding bit is given "0".
2. If PortB.x ODN configuration is selected, the corresponding data bit of \$0A should be set as "0". Therefore, it outputs low. It will be configured as floating state if the corresponding bit is given "1".
3. The attribution setting of PortC and PortD are similar to PortB.

7. UART

The speed rate of UART (Universal Asynchronous Receiver and Transmitter) supports up to 115.2kbps. The UART operation is controlled by UART Command Registers, \$19 and \$1A. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be set in command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt asserts when a byte is received or transmitted. By reading the Status Register, \$1A, user knows whether the interrupt is generated by Rx or Tx. Framing, overrun and parity errors are detected whenever every byte is received. All error status can be read from Status Register, \$1A.

The UART supports clock auto calibration. If auto-calibration is selected, standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to Baud Rate Control Registers, \$1E and \$1F. The following table depicts the relationships between baud rate and minimum Fosc requirement.

Baud Rate	High Byte (\$1F)	Low Byte (\$1E)	Min. Fosc
1200	00H	4BH	24000
2400	00H	96H	48000
4800	01H	2CH	96000
9600	02H	58H	192000
19200	04H	B0H	384000
38400	09H	60H	768000
51200	0CH	80H	1024000
57600	0EH	10H	1152000
102400	19H	00H	2048000
115200	1CH	20H	2304000

Note:

1. When SCLK1 \neq 0 and SCLK0 \neq 0, the baud rate is decided by Baud Rate=Clock Source/M where M is the value loaded into Port\$1C (low byte) and Port\$1D (high byte).
2. While using UART, the b6 and b7 of \$01(IRQ), and b6 and b7 of \$1A (UART_Command2) must be enabled.
3. While using UART with interrupt method for data transferring, b6 and b7 of \$19 (UART_Command1) must be enabled. In contrast, b6 and b7 of \$19 do not have to be enabled while using UART with polling method.
4. When Rx is applied, PortC.3 should be declared as input pull high to make sure that Rx interrupt is triggered (logic low level trigger) by the external signal. Otherwise, Rx interrupt may be always occurred.

If the auto-calibration is not selected, users can get desired baud rates by writing appropriate values to Pre-Scalar Registers, \$1C and \$1D. Non-standard baud rates can be obtained in this method. While using non-calibration mode, one should be aware of that the frequency of R-oscillator might alter due to the following factors:

1. Manufacturing process variations
2. Power supply
3. Operating temperature
4. Tolerance of external R components

7.1. P_19H_UART_Command1 (\$19H) (W) (Default: 00H)

P_UART_Command1		0x19			UART Interrupt/Parity Check Control			
Bit	7	6	5	4	3	2	1	0
Function	RxIntEn	TxIntEn	I_Reset	-	Parity	P_Check	SCLK1	SCLK0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RxIntEn	W	Receiver Interrupt Enable	0= disable 1= enable
6	TxIntEn	W	Transmitter Interrupt Enable	0= disable 1= enable
5	I_Reset	W	Internal Reset	1=Internal Reset
3	Parity	W	Odd/Even parity check	0=Odd 1=Even
2	P_Check	W	Enable/Disable parity check	0= disable 1= enable
1 : 0	SCLK	W	Clock source selection	00= Frosc (auto calibrate clock, \$1E & \$1F must be set, 32768 mask option must be crystal) 01= 32768Hz(no auto calibrate clock, \$1C & \$1D must be set, B.R.= 32768/M) 10= reserved 11= clock source Frosc(no auto calibrate clock, \$1C & \$1D must be set, M=\$1C+\$1D,B.R.= Frosc/M)

7.2. P_1AH_UART_Command2 (\$1A) (W) (Default: 11000000)

P_UART_Command2		0x1A			UART Receive/Transmit Control			
Bit	7	6	5	4	3	2	1	0
Function	RxPinEn	TxPinEn	-	-	-	-	-	-
Default	1	1	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RxPinEn	W	Enable/Disable Receiving Pin	0= disable 1= enable
6	TxPinEn	W	Enable/Disable Transmitting Pin	0= disable 1= enable

7.3. P_1AH_UART_Status (\$1A)(R)

P_UART_Status		0x1A			Read UART Status			
Bit	7	6	5	4	3	2	1	0
Function	RxRDY	TxRDY	FE	OE	PE	-	-	AcRDY
Default	0	1	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RxRDY	R	Data is received or not. When this bit is 1, you can read UART data.	0= not received 1= received
6	TxRDY	R	Transmitter ready or not	0= not ready 1= ready
5	FE	R	Sop bit is not detected; it means Frame error.	0= no error 1= error
4	OE	R	Overrun error means CPU does not read UART data before next one is available.	0= no error 1= error
3	PE	R	Parity check error.	0= no error 1= error
0	AcRDY	R	AC_clock wave form(auto calibrate clock) is ready or not.	0= not ready 1= ready

7.4. P_1BH_UART_Data (\$1B) (R/W)

P_UART_Data		0x1B			UART Data Port			
Bit	7	6	5	4	3	2	1	0
Function	UART Data							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	UART Data	R/W	UART Data	

7.5. P_1EH_UART_BaudRate_Low (\$1E)

P_UART_BaudRate_Low		0x1E			UART BaudRate Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	UART BaudRate							
Default	1	0	1	1	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	UART Baudrate	R/W	If auto-calibration is selected, standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to Baud Rate Control Registers, \$1E and \$1F.	

7.6. P_1FH_UART_BaudRate_High (\$1F)

P_UART_BaudRate_High			0X1F		UART BaudRate High Byte			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	UART BaudRate				
Default	0	0	0	0	0	1	0	0

Bit	Function	Type	Description	Condition
7 : 0	UART Baudrate	R/W	If auto-calibration is selected, standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to Baud Rate Control Registers, \$1E and \$1F	

\$1E & \$1F default baud rate = 19200

7.7. P_1CH_BaudScalar_Low (\$1C)

P_UART_BaudScalar_Low			0x1C		UART BaudScalar Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	UART BaudScalar							
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	UART BaudScalar	R/W	When SCLK1 \neq 0 and SCLK0 \neq 0, the baud rate is decided by Baud Rate=Clock Source/M where M is the value loaded into Port\$1C (low byte) and Port\$1D (high byte).	

X: Unknow

7.8. P_1DH_BaudScalar_High (\$1D)

P_UART_BaudScalar_High			0X1D		UART BaudScalar High Byte			
Bit	7	6	5	4	3	2	1	0
Function	UART BaudScalar							
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	UART BaudScalar	R/W	When SCLK1 \neq 0 and SCLK0 \neq 0, the baud rate is decided by Baud Rate=Clock Source/M where M is the value loaded into Port\$1C (low byte) and Port\$1D (high byte).	

X: Unknow

7.9. UART Program Example

```

;=====
;UART Program Example
;=====

```

```

T_UART_1FH_TABLE:
    DB    00h, 00h, 01h, 02h, 04h, 09h, 0Ch, 0Eh, 19h, 1Ch
T_UART_1EH_TABLE:
    DB    4Bh, 96h, 2Ch, 58h, B0h, 60h, 80h, 10h, 00h, 20h

```

; To Execute this Program correctly, interconnect P3.7(RX) and P3.5(TX)

```

    LDX    #0                ; Baud Rate Mode Index!
    SEI
    LDA    #%00100000        ;
    STA    P_19H_UART_Command1 ; Reset UART
    LDA    #%11000000        ;
    STA    P_19H_UART_Command1 ; enable Tx and Rx IRQ
    STA    P_1AH_UART_Command2 ; enable Tx and Rx
    LDA    T_UART_1EH_TABLE,X
    STA    $1EH
    LDA    T_UART_1FH_TABLE,X ; Baud rate Setup
    STA    $1FH

L_WaitClockReady:           ; Wait Auto Calibrate Clock Ready
    LDA    P_1AH_UART_Command2
    AND    #%00000001
    BEQ    L_WaitClockReady
    LDA    #%11111111
    STA    P_02H_InterruptClear
    LDA    #%11000000
    STA    R_InterruptImage
    STA    P_01H_InterruptControl
    CLI
    LDY    #0

L_DataLoop:

L_WaitTXReady:
    BIT    P_1AH_UART_Command2 ; Polling Data Transmit Ok flag
    BVC    L_WaitTXReady
    LDA    T_TXRXPattern,Y      ; Output Data to TX_RX port
    STA    P_1BH_ReceiveTransmitData

L_WaitRXReady:
    LDA    P_1AH_UART_Command2 ; Polling Data Receive Ready flag
    BPL    L_WaitRXReady
    LDA    P_ReceiveTransmitData ; Receive from TX_RX port
    CMP    T_TXRXPattern,Y
    BNE    L_TXRXError
    INY
    CPY    #D_NumberofTXData
    BNE    L_DataLoop

```

8. PWM/DAC Audio Driver

The GPLB3X offers one pair of PWM (Pulse Width Modulation) drivers. The GPLB32/37 provides both PWM and DAC drivers, which can be selected by mask option. Both PWM and DAC drivers support two sound channels. Each channel is able to play speech or tone individually. The PWM driver is able to drive speaker or buzzer directly without any buffer or amplification circuit. In DAC mode, the audio driver can be amplified by a bipolar-transistor or amplifier to drive a speaker or a buzzer.

8.1. P_12H_Ch0_PWM_DAC_Ctrl (\$12) (W) (Default: 00000000)

P_Ch0_PWM_DAC_Ctrl	0x12		PWM/DAC Ch0 Control and Select PWM/DAC for Speech/Tone					
Bit	7	6	5	4	3	2	1	0
Function	CHE0	SP/T	-	DACL1	DACL0	-	-	-
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CHE0	W	Enable/Disable PWM/DAC Ch0 Note: In DAC mode, the \$12.7 must be set to "0" after end of audio play or before sleep entrance. Otherwise, it will cause a 5mA current consumption once the \$12.7 is set to "1" even though the DAC output (\$13) ramps down to 0.	0= disable 1= enable
		R	Read Ch0 PWM/DAC Status	
6	CP/T	W	Select Ch0 for Speech or Tone	0= speech
		R	Read Ch0 sound type	1= tone
4 : 3	DACL	W	Timing for Channel0 data to PWM/DAC Note: In tone mode, "0" must be given in b4 and b3 Note: PWM Ch0 frequency is determined by Timer0.	00= directly 01= after timer0 overflows 10= after timer1 overflows
		R	Read timing for Channel0 data to PWM/DAC	11= after timer0 or timer1 overflows

8.2. P_16H_Ch1_PWM_DAC_Ctrl (\$16) (W) (Default: 00000000)

P_Ch1_PWM_DAC_Ctrl	0x16		PWM/DAC Ch1 Control and Select PWM/DAC for Speech/Tone					
Bit	7	6	5	4	3	2	1	0
Function	CHE1	SP/T	-	DACH1	DACH0	-	-	-
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CHE1	W	Enable/Disable PWM/DAC Ch1 Note: In DAC mode, the \$16.7 must be set to "0" after end of audio play or before sleep entrance. Otherwise, it will cause a 5mA current consumption once the \$16.7 is set to "1" even though the DAC output (\$17) ramps down to 0.	0= disable 1= enable
		R	Read Ch1 PWM/DAC Status	
6	SP/T	W	Select Ch1 for Speech or Tone	0= speech
		R	Read Ch1 sound type	1= tone
4 : 3	DACL	W	Timing for Channel1 data to PWM/DAC Note: In tone mode, "0" must be given in b4 and b3. Note: PWM Ch1 frequency is determined by Timer1.	00= directly 01= after timer0 overflows 10= after timer1 overflows
		R	Read timing for Channel1 data to PWM/DAC	11= after timer0 or timer1 overflows

8.3. P_13H_Ch0_PWM_DAC_Output (\$13) (W)

P_Ch0_PWM_DAC_Output		0x13			Ch0 Output Data			
Bit	7	6	5	4	3	2	1	0
Function	Ch0 Speech/Tone Data							
Default	X-	X	X	X	X	X	X	X

X: Unknown

Bit	Function	Type	Description	Condition
7 : 0	Speech/Tone Data	W	Write Ch0 Speech/Tone data 1. In tone mode , \$13H = volume control , \$13H =00H (Min volume), \$13H = 7FH (Max volume). 2. Switch tone mode on as follows. STEP1. select tone mode. SETP2. sett volume. 3. If step2 is performed prior to step1, the volume is unknown .	

Write to output speech/tone envelope.

8.4. P_17H_Ch1_PWM_DAC_Output (\$17) (W)

P_Ch1_PWM_DAC_Output		0x17			Ch1 Output Data			
Bit	7	6	5	4	3	2	1	0
Function	Ch1 Speech/Tone Data							
Default	X-	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	Speech/Tone Data	W	Write Ch1 Speech/Tone data 1. In tone mode , \$17H = volume control , \$17H = 00H (Min volume), \$17H = 7FH (Max volume). 2. Switch tone mode on as follows. STEP1. select tone mode. SETP2. setting volume. 3. If step2 is performed prior to step1, the volume is unknown .	

Write to output speech/tone envelope. In tone mode, it is a volume control port.

9. LCD Buffer RAM (DPRAM)

9.1. LCD Address Mapping for GPLB30/31/32/34/37

Body	Com x Seg
GPLB30:	16 x 70
GPLB31:	32 x 74
GPLB32/37:	16 x 74, 32 x 64
GPLB34:	32 x 74

	S0-S7	S8-S15	S16-S23	S24-S31	S32-S39	S40-S47	S48-S55	S56-S63	S64-S71	S72-S73
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b1
Com0	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05	\$3E06	\$3E07	\$3E08	\$3E09
Com1	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15	\$3E16	\$3E17	\$3E18	\$3E19
Com2	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25	\$3E26	\$3E27	\$3E28	\$3E29
Com3	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35	\$3E36	\$3E37	\$3E38	\$3E39
Com4	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45	\$3E46	\$3E47	\$3E48	\$3E49
Com5	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55	\$3E56	\$3E57	\$3E58	\$3E59
Com6	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65	\$3E66	\$3E67	\$3E68	\$3E69
Com7	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75	\$3E76	\$3E77	\$3E78	\$3E79
Com8	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85	\$3E86	\$3E87	\$3E88	\$3E89
Com9	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95	\$3E96	\$3E97	\$3E98	\$3E99
Com10	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5	\$3EA6	\$3EA7	\$3EA8	\$3EA9
Com11	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5	\$3EB6	\$3EB7	\$3EB8	\$3EB9
Com12	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5	\$3EC6	\$3EC7	\$3EC8	\$3EC9
Com13	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5	\$3ED6	\$3ED7	\$3ED8	\$3ED9
Com14	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5	\$3EE6	\$3EE7	\$3EE8	\$3EE9
Com15	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5	\$3EF6	\$3EF7	\$3EF8	\$3EF9
Com16	\$3F00	\$3F01	\$3F02	\$3F03	\$3F04	\$3F05	\$3F06	\$3F07	\$3F08	\$3F09
Com17	\$3F10	\$3F11	\$3F12	\$3F13	\$3F14	\$3F15	\$3F16	\$3F17	\$3F18	\$3F19
Com18	\$3F20	\$3F21	\$3F22	\$3F23	\$3F24	\$3F25	\$3F26	\$3F27	\$3F28	\$3F29
Com19	\$3F30	\$3F31	\$3F32	\$3F33	\$3F34	\$3F35	\$3F36	\$3F37	\$3F38	\$3F39
Com20	\$3F40	\$3F41	\$3F42	\$3F43	\$3F44	\$3F45	\$3F46	\$3F47	\$3F48	\$3F49
Com21	\$3F50	\$3F51	\$3F52	\$3F53	\$3F54	\$3F55	\$3F56	\$3F57	\$3F58	\$3F59
Com22	\$3F60	\$3F61	\$3F62	\$3F63	\$3F64	\$3F65	\$3F66	\$3F67	\$3F68	\$3F69
Com23	\$3F70	\$3F71	\$3F72	\$3F73	\$3F74	\$3F75	\$3F76	\$3F77	\$3F78	\$3F79
Com24	\$3F80	\$3F81	\$3F82	\$3F83	\$3F84	\$3F85	\$3F86	\$3F87	\$3F88	\$3F89
Com25	\$3F90	\$3F91	\$3F92	\$3F93	\$3F94	\$3F95	\$3F96	\$3F97	\$3F98	\$3F99
Com26	\$3FA0	\$3FA1	\$3FA2	\$3FA3	\$3FA4	\$3FA5	\$3FA6	\$3FA7	\$3FA8	\$3FA9
Com27	\$3FB0	\$3FB1	\$3FB2	\$3FB3	\$3FB4	\$3FB5	\$3FB6	\$3FB7	\$3FB8	\$3FB9
Com28	\$3FC0	\$3FC1	\$3FC2	\$3FC3	\$3FC4	\$3FC5	\$3FC6	\$3FC7	\$3FC8	\$3FC9
Com29	\$3FD0	\$3FD1	\$3FD2	\$3FD3	\$3FD4	\$3FD5	\$3FD6	\$3FD7	\$3FD8	\$3FD9
Com30	\$3FE0	\$3FE1	\$3FE2	\$3FE3	\$3FE4	\$3FE5	\$3FE6	\$3FE7	\$3FE8	\$3FE9
Com31	\$3FF0	\$3FF1	\$3FF2	\$3FF3	\$3FF4	\$3FF5	\$3FF6	\$3FF7	\$3FF8	\$3FF9

9.2. LCD Address Mapping for GPLB33A: 16x52

	S0-S7	S8-S15	S16-S23	S24-S31	S32-S39	S40-S47	S48-S51
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b3
Com0	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05	\$3E06
Com1	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15	\$3E16
Com2	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25	\$3E26
Com3	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35	\$3E36
Com4	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45	\$3E46
Com5	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55	\$3E56
Com6	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65	\$3E66
Com7	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75	\$3E76
Com8	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85	\$3E86
Com9	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95	\$3E96
Com10	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5	\$3EA6
Com11	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5	\$3EB6
Com12	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5	\$3EC6
Com13	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5	\$3ED6
Com14	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5	\$3EE6
Com15	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5	\$3EF6

9.3. LCD Address Mapping for GPLB33B: 16x48

	S0-S7	S8-S15	S16-S23	S24-S31	S32-S39	S40-S47
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7
Com0	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05
Com1	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15
Com2	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25
Com3	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35
Com4	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45
Com5	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55
Com6	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65
Com7	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75
Com8	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85
Com9	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95
Com10	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5
Com11	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5
Com12	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5
Com13	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5
Com14	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5
Com15	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5

9.4. LCD Address Mapping for GPLB35/36: 16x100, 32x100, 36x96, 48x84

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95	S96- S99
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b3
Com0	\$3D00	\$3D01	\$3D02	\$3D03	\$3D04	\$3D05	\$3D06	\$3D07	\$3D08	\$3D09	\$3D0A	\$3D0B	\$3D0C
Com1	\$3D10	\$3D11	\$3D12	\$3D13	\$3D14	\$3D15	\$3D16	\$3D17	\$3D18	\$3D19	\$3D1A	\$3D1B	\$3D1C
Com2	\$3D20	\$3D21	\$3D22	\$3D23	\$3D24	\$3D25	\$3D26	\$3D27	\$3D28	\$3D29	\$3D2A	\$3D2B	\$3D2C
Com3	\$3D30	\$3D31	\$3D32	\$3D33	\$3D34	\$3D35	\$3D36	\$3D37	\$3D38	\$3D39	\$3D3A	\$3D3B	\$3D3C
Com4	\$3D40	\$3D41	\$3D42	\$3D43	\$3D44	\$3D45	\$3D46	\$3D47	\$3D48	\$3D49	\$3D4A	\$3D4B	\$3D4C
Com5	\$3D50	\$3D51	\$3D52	\$3D53	\$3D54	\$3D55	\$3D56	\$3D57	\$3D58	\$3D59	\$3D5A	\$3D5B	\$3D5C
Com6	\$3D60	\$3D61	\$3D62	\$3D63	\$3D64	\$3D65	\$3D66	\$3D67	\$3D68	\$3D69	\$3D6A	\$3D6B	\$3D6C
Com7	\$3D70	\$3D71	\$3D72	\$3D73	\$3D74	\$3D75	\$3D76	\$3D77	\$3D78	\$3D79	\$3D7A	\$3D7B	\$3D7C
Com8	\$3D80	\$3D81	\$3D82	\$3D83	\$3D84	\$3D85	\$3D86	\$3D87	\$3D88	\$3D89	\$3D8A	\$3D8B	\$3D8C
Com9	\$3D90	\$3D91	\$3D92	\$3D93	\$3D94	\$3D95	\$3D96	\$3D97	\$3D98	\$3D99	\$3D9A	\$3D9B	\$3D9C
Com10	\$3DA0	\$3DA1	\$3DA2	\$3DA3	\$3DA4	\$3DA5	\$3DA6	\$3DA7	\$3DA8	\$3DA9	\$3DAA	\$3DAB	\$3DAC
Com11	\$3DB0	\$3DB1	\$3DB2	\$3DB3	\$3DB4	\$3DB5	\$3DB6	\$3DB7	\$3DB8	\$3DB9	\$3DBA	\$3DBB	\$3DBC
Com12	\$3DC0	\$3DC1	\$3DC2	\$3DC3	\$3DC4	\$3DC5	\$3DC6	\$3DC7	\$3DC8	\$3DC9	\$3DCA	\$3DCB	\$3DCC
Com13	\$3DD0	\$3DD1	\$3DD2	\$3DD3	\$3DD4	\$3DD5	\$3DD6	\$3DD7	\$3DD8	\$3DD9	\$3DDA	\$3ddb	\$3DDC
Com14	\$3DE0	\$3DE1	\$3DE2	\$3DE3	\$3DE4	\$3DE5	\$3DE6	\$3DE7	\$3DE8	\$3DE9	\$3DEA	\$3DEB	\$3DEC
Com15	\$3DF0	\$3DF1	\$3DF2	\$3DF3	\$3DF4	\$3DF5	\$3DF6	\$3DF7	\$3DF8	\$3DF9	\$3DFA	\$3DFB	\$3DFC
Com16	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05	\$3E06	\$3E07	\$3E08	\$3E09	\$3E0A	\$3E0B	\$3E0C
Com17	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15	\$3E16	\$3E17	\$3E18	\$3E19	\$3E1A	\$3E1B	\$3E1C
Com18	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25	\$3E26	\$3E27	\$3E28	\$3E29	\$3E2A	\$3E2B	\$3E2C
Com19	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35	\$3E36	\$3E37	\$3E38	\$3E39	\$3E3A	\$3E3B	\$3E3C
Com20	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45	\$3E46	\$3E47	\$3E48	\$3E49	\$3E4A	\$3E4B	\$3E4C
Com21	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55	\$3E56	\$3E57	\$3E58	\$3E59	\$3E5A	\$3E5B	\$3E5C
Com22	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65	\$3E66	\$3E67	\$3E68	\$3E69	\$3E6A	\$3E6B	\$3E6C
Com23	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75	\$3E76	\$3E77	\$3E78	\$3E79	\$3E7A	\$3E7B	\$3E7C
Com24	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85	\$3E86	\$3E87	\$3E88	\$3E89	\$3E8A	\$3E8B	\$3E8C
Com25	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95	\$3E96	\$3E97	\$3E98	\$3E99	\$3E9A	\$3E9B	\$3E9C
Com26	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5	\$3EA6	\$3EA7	\$3EA8	\$3EA9	\$3EAA	\$3EAB	\$3EAC
Com27	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5	\$3EB6	\$3EB7	\$3EB8	\$3EB9	\$3EBA	\$3EBB	\$3EBC
Com28	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5	\$3EC6	\$3EC7	\$3EC8	\$3EC9	\$3ECA	\$3ECB	\$3ECC
Com29	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5	\$3ED6	\$3ED7	\$3ED8	\$3ED9	\$3EDA	\$3EDB	\$3EDC
Com30	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5	\$3EE6	\$3EE7	\$3EE8	\$3EE9	\$3EEA	\$3EEB	\$3EEC
Com31	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5	\$3EF6	\$3EF7	\$3EF8	\$3EF9	\$3EFA	\$3EFB	\$3EFC
Com32	\$3F00	\$3F01	\$3F02	\$3F03	\$3F04	\$3F05	\$3F06	\$3F07	\$3F08	\$3F09	\$3F0A	\$3F0B	\$3F0C
Com33	\$3F10	\$3F11	\$3F12	\$3F13	\$3F14	\$3F15	\$3F16	\$3F17	\$3F18	\$3F19	\$3F1A	\$3F1B	\$3F1C
Com34	\$3F20	\$3F21	\$3F22	\$3F23	\$3F24	\$3F25	\$3F26	\$3F27	\$3F28	\$3F29	\$3F2A	\$3F2B	\$3F2C
Com35	\$3F30	\$3F31	\$3F32	\$3F33	\$3F34	\$3F35	\$3F36	\$3F37	\$3F38	\$3F39	\$3F3A	\$3F3B	\$3F3C
Com36	\$3F40	\$3F41	\$3F42	\$3F43	\$3F44	\$3F45	\$3F46	\$3F47	\$3F48	\$3F49	\$3F4A	\$3F4B	\$3F4C
Com37	\$3F50	\$3F51	\$3F52	\$3F53	\$3F54	\$3F55	\$3F56	\$3F57	\$3F58	\$3F59	\$3F5A	\$3F5B	\$3F5C

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95	S96- S99
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b3
Com38	\$3F60	\$3F61	\$3F62	\$3F63	\$3F64	\$3F65	\$3F66	\$3F67	\$3F68	\$3F69	\$3F6A	\$3F6B	\$3F6C
Com39	\$3F70	\$3F71	\$3F72	\$3F73	\$3F74	\$3F75	\$3F76	\$3F77	\$3F78	\$3F79	\$3F7A	\$3F7B	\$3F7C
Com40	\$3F80	\$3F81	\$3F82	\$3F83	\$3F84	\$3F85	\$3F86	\$3F87	\$3F88	\$3F89	\$3F8A	\$3F8B	\$3F8C
Com41	\$3F90	\$3F91	\$3F92	\$3F93	\$3F94	\$3F95	\$3F96	\$3F97	\$3F98	\$3F99	\$3F9A	\$3F9B	\$3F9C
Com42	\$3FA0	\$3FA1	\$3FA2	\$3FA3	\$3FA4	\$3FA5	\$3FA6	\$3FA7	\$3FA8	\$3FA9	\$3FAA	\$3FAB	\$3FAC
Com43	\$3FB0	\$3FB1	\$3FB2	\$3FB3	\$3FB4	\$3FB5	\$3FB6	\$3FB7	\$3FB8	\$3FB9	\$3FBA	\$3FBB	\$3FBC
Com44	\$3FC0	\$3FC1	\$3FC2	\$3FC3	\$3FC4	\$3FC5	\$3FC6	\$3FC7	\$3FC8	\$3FC9	\$3FCA	\$3FCB	\$3FC
Com45	\$3FD0	\$3FD1	\$3FD2	\$3FD3	\$3FD4	\$3FD5	\$3FD6	\$3FD7	\$3FD8	\$3FD9	\$3FDA	\$3FDB	\$3FDC
Com46	\$3FE0	\$3FE1	\$3FE2	\$3FE3	\$3FE4	\$3FE5	\$3FE6	\$3FE7	\$3FE8	\$3FE9	\$3FEA	\$3FEB	\$3FEC
Com47	\$3FF0	\$3FF1	\$3FF2	\$3FF3	\$3FF4	\$3FF5	\$3FF6	\$3FF7	\$3FF8	\$3FF9	\$3FFA	\$3FFB	\$3FFC

9.5. LCD Address Mapping for GPLB39: 64x96

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95		
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b3
Com0	\$3C00	\$3C01	\$3C02	\$3C03	\$3C04	\$3C05	\$3C06	\$3C07	\$3C08	\$3C09	\$3C0A	\$3C0B	\$3C0C	\$3C0D
Com1	\$3C10	\$3C11	\$3C12	\$3C13	\$3C14	\$3C15	\$3C16	\$3C17	\$3C18	\$3C19	\$3C1A	\$3C1B	\$3C1C	\$3C1D
Com2	\$3C20	\$3C21	\$3C22	\$3C23	\$3C24	\$3C25	\$3C26	\$3C27	\$3C28	\$3C29	\$3C2A	\$3C2B	\$3C2C	\$3C2D
Com3	\$3C30	\$3C31	\$3C32	\$3C33	\$3C34	\$3C35	\$3C36	\$3C37	\$3C38	\$3C39	\$3C3A	\$3C3B	\$3C3C	\$3C3C
Com4	\$3C40	\$3C41	\$3C42	\$3C43	\$3C44	\$3C45	\$3C46	\$3C47	\$3C48	\$3C49	\$3C4A	\$3C4B	\$3C4C	\$3C4D
Com5	\$3C50	\$3C51	\$3C52	\$3C53	\$3C54	\$3C55	\$3C56	\$3C57	\$3C58	\$3C59	\$3C5A	\$3C5B	\$3C5C	\$3C5D
Com6	\$3C60	\$3C61	\$3C62	\$3C63	\$3C64	\$3C65	\$3C66	\$3C67	\$3C68	\$3C69	\$3C6A	\$3C6B	\$3C6C	\$3C6D
Com7	\$3C70	\$3C71	\$3C72	\$3C73	\$3C74	\$3C75	\$3C76	\$3C77	\$3C78	\$3C79	\$3C7A	\$3C7B	\$3C7C	\$3C7D
Com8	\$3C80	\$3C81	\$3C82	\$3C83	\$3C84	\$3C85	\$3C86	\$3C87	\$3C88	\$3C89	\$3C8A	\$3C8B	\$3C8C	\$3C8D
Com9	\$3C90	\$3C91	\$3C92	\$3C93	\$3C94	\$3C95	\$3C96	\$3C97	\$3C98	\$3C99	\$3C9A	\$3C9B	\$3C9C	\$3C9D
Com10	\$3CA0	\$3CA1	\$3CA2	\$3CA3	\$3CA4	\$3CA5	\$3CA6	\$3CA7	\$3CA8	\$3CA9	\$3CAA	\$3CAB	\$3CAC	\$3CAD
Com11	\$3CB0	\$3CB1	\$3CB2	\$3CB3	\$3CB4	\$3CB5	\$3CB6	\$3CB7	\$3CB8	\$3CB9	\$3CBA	\$3CBB	\$3CBC	\$3CBD
Com12	\$3CC0	\$3CC1	\$3CC2	\$3CC3	\$3CC4	\$3CC5	\$3CC6	\$3CC7	\$3CC8	\$3CC9	\$3CCA	\$3CCB	\$3CCC	\$3CCD
Com13	\$3CD0	\$3CD1	\$3CD2	\$3CD3	\$3CD4	\$3CD5	\$3CD6	\$3CD7	\$3CD8	\$3CD9	\$3CDA	\$3CDB	\$3CDC	\$3CDD
Com14	\$3CE0	\$3CE1	\$3CE2	\$3CE3	\$3CE4	\$3CE5	\$3CE6	\$3CE7	\$3CE8	\$3CE9	\$3CEA	\$3CEB	\$3CEC	\$3CED
Com15	\$3CF0	\$3CF1	\$3CF2	\$3CF3	\$3CF4	\$3CF5	\$3CF6	\$3CF7	\$3CF8	\$3CF9	\$3CFA	\$3CFB	\$3CFC	\$3CFD
Com16	\$3D00	\$3D01	\$3D02	\$3D03	\$3D04	\$3D05	\$3D06	\$3D07	\$3D08	\$3D09	\$3D0A	\$3D0B	\$3D0C	\$3D0D
Com17	\$3D10	\$3D11	\$3D12	\$3D13	\$3D14	\$3D15	\$3D16	\$3D17	\$3D18	\$3D19	\$3D1A	\$3D1B	\$3D1C	\$3D1D
Com18	\$3D20	\$3D21	\$3D22	\$3D23	\$3D24	\$3D25	\$3D26	\$3D27	\$3D28	\$3D29	\$3D2A	\$3D2B	\$3D2C	\$3D2D
Com19	\$3D30	\$3D31	\$3D32	\$3D33	\$3D34	\$3D35	\$3D36	\$3D37	\$3D38	\$3D39	\$3D3A	\$3D3B	\$3D3C	\$3D3D
Com20	\$3D40	\$3D41	\$3D42	\$3D43	\$3D44	\$3D45	\$3D46	\$3D47	\$3D48	\$3D49	\$3D4A	\$3D4B	\$3D4C	\$3D4D
Com21	\$3D50	\$3D51	\$3D52	\$3D53	\$3D54	\$3D55	\$3D56	\$3D57	\$3D58	\$3D59	\$3D5A	\$3D5B	\$3D5C	\$3D5D
Com22	\$3D60	\$3D61	\$3D62	\$3D63	\$3D64	\$3D65	\$3D66	\$3D67	\$3D68	\$3D69	\$3D6A	\$3D6B	\$3D6C	\$3D6D
Com23	\$3D70	\$3D71	\$3D72	\$3D73	\$3D74	\$3D75	\$3D76	\$3D77	\$3D78	\$3D79	\$3D7A	\$3D7B	\$3D7C	\$3D7D



	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95		
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b3
Com24	\$3D80	\$3D81	\$3D82	\$3D83	\$3D84	\$3D85	\$3D86	\$3D87	\$3D88	\$3D89	\$3D8A	\$3D8B	\$3D8C	\$3D8D
Com25	\$3D90	\$3D91	\$3D92	\$3D93	\$3D94	\$3D95	\$3D96	\$3D97	\$3D98	\$3D99	\$3D9A	\$3D9B	\$3D9C	\$3D9D
Com26	\$3DA0	\$3DA1	\$3DA2	\$3DA3	\$3DA4	\$3DA5	\$3DA6	\$3DA7	\$3DA8	\$3DA9	\$3DAA	\$3DAB	\$3DAC	\$3DAD
Com27	\$3DB0	\$3DB1	\$3DB2	\$3DB3	\$3DB4	\$3DB5	\$3DB6	\$3DB7	\$3DB8	\$3DB9	\$3DBA	\$3DBB	\$3DBC	\$3DBD
Com28	\$3DC0	\$3DC1	\$3DC2	\$3DC3	\$3DC4	\$3DC5	\$3DC6	\$3DC7	\$3DC8	\$3DC9	\$3DCA	\$3DCB	\$3DCC	\$3DCD
Com29	\$3DD0	\$3DD1	\$3DD2	\$3DD3	\$3DD4	\$3DD5	\$3DD6	\$3DD7	\$3DD8	\$3DD9	\$3DDA	\$3ddb	\$3DDC	\$3DDD
Com30	\$3DE0	\$3DE1	\$3DE2	\$3DE3	\$3DE4	\$3DE5	\$3DE6	\$3DE7	\$3DE8	\$3DE9	\$3DEA	\$3DEB	\$3DEC	\$3DED
Com31	\$3DF0	\$3DF1	\$3DF2	\$3DF3	\$3DF4	\$3DF5	\$3DF6	\$3DF7	\$3DF8	\$3DF9	\$3DFA	\$3DFB	\$3DFC	\$3DFD
Com32	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05	\$3E06	\$3E07	\$3E08	\$3E09	\$3E0A	\$3E0B	\$3E0C	\$3E0D
Com33	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15	\$3E16	\$3E17	\$3E18	\$3E19	\$3E1A	\$3E1B	\$3E1C	\$3E1D
Com34	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25	\$3E26	\$3E27	\$3E28	\$3E29	\$3E2A	\$3E2B	\$3E2C	\$3E2D
Com35	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35	\$3E36	\$3E37	\$3E38	\$3E39	\$3E3A	\$3E3B	\$3E3C	\$3E3D
Com36	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45	\$3E46	\$3E47	\$3E48	\$3E49	\$3E4A	\$3E4B	\$3E4C	\$3E4D
Com37	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55	\$3E56	\$3E57	\$3E58	\$3E59	\$3E5A	\$3E5B	\$3E5C	\$3E5D
Com38	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65	\$3E66	\$3E67	\$3E68	\$3E69	\$3E6A	\$3E6B	\$3E6C	\$3E6D
Com39	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75	\$3E76	\$3E77	\$3E78	\$3E79	\$3E7A	\$3E7B	\$3E7C	\$3E7D
Com40	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85	\$3E86	\$3E87	\$3E88	\$3E89	\$3E8A	\$3E8B	\$3E8C	\$3E8D
Com41	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95	\$3E96	\$3E97	\$3E98	\$3E99	\$3E9A	\$3E9B	\$3E9C	\$3E9D
Com42	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5	\$3EA6	\$3EA7	\$3EA8	\$3EA9	\$3EAA	\$3EAB	\$3EAC	\$3EAD
Com43	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5	\$3EB6	\$3EB7	\$3EB8	\$3EB9	\$3EBA	\$3EBB	\$3EBC	\$3EBD
Com44	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5	\$3EC6	\$3EC7	\$3EC8	\$3EC9	\$3ECA	\$3ECB	\$3ECC	\$3ECD
Com45	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5	\$3ED6	\$3ED7	\$3ED8	\$3ED9	\$3EDA	\$3EDB	\$3EDC	\$3EDD
Com46	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5	\$3EE6	\$3EE7	\$3EE8	\$3EE9	\$3EEA	\$3EEB	\$3EEC	\$3EED
Com47	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5	\$3EF6	\$3EF7	\$3EF8	\$3EF9	\$3EFA	\$3EFB	\$3EFC	\$3EFD
Com48	\$3F00	\$3F01	\$3F02	\$3F03	\$3F04	\$3F05	\$3F06	\$3F07	\$3F08	\$3F09	\$3F0A	\$3F0B	\$3F0C	\$3F0D
Com49	\$3F10	\$3F11	\$3F12	\$3F13	\$3F14	\$3F15	\$3F16	\$3F17	\$3F18	\$3F19	\$3F1A	\$3F1B	\$3F1C	\$3F1D
Com50	\$3F20	\$3F21	\$3F22	\$3F23	\$3F24	\$3F25	\$3F26	\$3F27	\$3F28	\$3F29	\$3F2A	\$3F2B	\$3F2C	\$3F2D
Com51	\$3F30	\$3F31	\$3F32	\$3F33	\$3F34	\$3F35	\$3F36	\$3F37	\$3F38	\$3F39	\$3F3A	\$3F3B	\$3F3C	\$3F3D
Com52	\$3F40	\$3F41	\$3F42	\$3F43	\$3F44	\$3F45	\$3F46	\$3F47	\$3F48	\$3F49	\$3F4A	\$3F4B	\$3F4C	\$3F4D
Com53	\$3F50	\$3F51	\$3F52	\$3F53	\$3F54	\$3F55	\$3F56	\$3F57	\$3F58	\$3F59	\$3F5A	\$3F5B	\$3F5C	\$3F5D
Com54	\$3F60	\$3F61	\$3F62	\$3F63	\$3F64	\$3F65	\$3F66	\$3F67	\$3F68	\$3F69	\$3F6A	\$3F6B	\$3F6C	\$3F6D
Com55	\$3F70	\$3F71	\$3F72	\$3F73	\$3F74	\$3F75	\$3F76	\$3F77	\$3F78	\$3F79	\$3F7A	\$3F7B	\$3F7C	\$3F7D
Com56	\$3F80	\$3F81	\$3F82	\$3F83	\$3F84	\$3F85	\$3F86	\$3F87	\$3F88	\$3F89	\$3F8A	\$3F8B	\$3F8C	\$3F8D
Com57	\$3F90	\$3F91	\$3F92	\$3F93	\$3F94	\$3F95	\$3F96	\$3F97	\$3F98	\$3F99	\$3F9A	\$3F9B	\$3F9C	\$3F9D
Com58	\$3FA0	\$3FA1	\$3FA2	\$3FA3	\$3FA4	\$3FA5	\$3FA6	\$3FA7	\$3FA8	\$3FA9	\$3FAA	\$3FAB	\$3FAC	\$3FAD
Com59	\$3FB0	\$3FB1	\$3FB2	\$3FB3	\$3FB4	\$3FB5	\$3FB6	\$3FB7	\$3FB8	\$3FB9	\$3FBA	\$3FBB	\$3FBC	\$3FBD
Com60	\$3FC0	\$3FC1	\$3FC2	\$3FC3	\$3FC4	\$3FC5	\$3FC6	\$3FC7	\$3FC8	\$3FC9	\$3FCA	\$3FCB	\$3FCC	\$3FCD
Com61	\$3FD0	\$3FD1	\$3FD2	\$3FD3	\$3FD4	\$3FD5	\$3FD6	\$3FD7	\$3FD8	\$3FD9	\$3FDA	\$3FDB	\$3FDC	\$3FDD
Com62	\$3FE0	\$3FE1	\$3FE2	\$3FE3	\$3FE4	\$3FE5	\$3FE6	\$3FE7	\$3FE8	\$3FE9	\$3FEA	\$3FEB	\$3FEC	\$3FED
Com63	\$3FF0	\$3FF1	\$3FF2	\$3FF3	\$3FF4	\$3FF5	\$3FF6	\$3FF7	\$3FF8	\$3FF9	\$3FFA	\$3FFB	\$3FFC	\$3FFD

9.6. LCD Address Mapping for GPLB39: 48x112

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95	S96- S103	S104- S111
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7
Com0	\$3D00	\$3D01	\$3D02	\$3D03	\$3D04	\$3D05	\$3D06	\$3D07	\$3D08	\$3D09	\$3D0A	\$3D0B	\$3D0C	\$3D0D
Com1	\$3D10	\$3D11	\$3D12	\$3D13	\$3D14	\$3D15	\$3D16	\$3D17	\$3D18	\$3D19	\$3D1A	\$3D1B	\$3D1C	\$3D1D
Com2	\$3D20	\$3D21	\$3D22	\$3D23	\$3D24	\$3D25	\$3D26	\$3D27	\$3D28	\$3D29	\$3D2A	\$3D2B	\$3D2C	\$3D2D
Com3	\$3D30	\$3D31	\$3D32	\$3D33	\$3D34	\$3D35	\$3D36	\$3D37	\$3D38	\$3D39	\$3D3A	\$3D3B	\$3D3C	\$3D3D
Com4	\$3D40	\$3D41	\$3D42	\$3D43	\$3D44	\$3D45	\$3D46	\$3D47	\$3D48	\$3D49	\$3D4A	\$3D4B	\$3D4C	\$3D4D
Com5	\$3D50	\$3D51	\$3D52	\$3D53	\$3D54	\$3D55	\$3D56	\$3D57	\$3D58	\$3D59	\$3D5A	\$3D5B	\$3D5C	\$3D5D
Com6	\$3D60	\$3D61	\$3D62	\$3D63	\$3D64	\$3D65	\$3D66	\$3D67	\$3D68	\$3D69	\$3D6A	\$3D6B	\$3D6C	\$3D6D
Com7	\$3D70	\$3D71	\$3D72	\$3D73	\$3D74	\$3D75	\$3D76	\$3D77	\$3D78	\$3D79	\$3D7A	\$3D7B	\$3D7C	\$3D7D
Com8	\$3D80	\$3D81	\$3D82	\$3D83	\$3D84	\$3D85	\$3D86	\$3D87	\$3D88	\$3D89	\$3D8A	\$3D8B	\$3D8C	\$3D8D
Com9	\$3D90	\$3D91	\$3D92	\$3D93	\$3D94	\$3D95	\$3D96	\$3D97	\$3D98	\$3D99	\$3D9A	\$3D9B	\$3D9C	\$3D9D
Com10	\$3DA0	\$3DA1	\$3DA2	\$3DA3	\$3DA4	\$3DA5	\$3DA6	\$3DA7	\$3DA8	\$3DA9	\$3DAA	\$3DAB	\$3DAC	\$3DAD
Com11	\$3DB0	\$3DB1	\$3DB2	\$3DB3	\$3DB4	\$3DB5	\$3DB6	\$3DB7	\$3DB8	\$3DB9	\$3DBA	\$3DBB	\$3DBC	\$3DBD
Com12	\$3DC0	\$3DC1	\$3DC2	\$3DC3	\$3DC4	\$3DC5	\$3DC6	\$3DC7	\$3DC8	\$3DC9	\$3DCA	\$3DCB	\$3DCC	\$3DCD
Com13	\$3DD0	\$3DD1	\$3DD2	\$3DD3	\$3DD4	\$3DD5	\$3DD6	\$3DD7	\$3DD8	\$3DD9	\$3DDA	\$3ddb	\$3DDC	\$3DDD
Com14	\$3DE0	\$3DE1	\$3DE2	\$3DE3	\$3DE4	\$3DE5	\$3DE6	\$3DE7	\$3DE8	\$3DE9	\$3DEA	\$3DEB	\$3DEC	\$3DED
Com15	\$3DF0	\$3DF1	\$3DF2	\$3DF3	\$3DF4	\$3DF5	\$3DF6	\$3DF7	\$3DF8	\$3DF9	\$3DFA	\$3DFB	\$3DFC	\$3DFD
Com16	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05	\$3E06	\$3E07	\$3E08	\$3E09	\$3E0A	\$3E0B	\$3E0C	\$3E0D
Com17	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15	\$3E16	\$3E17	\$3E18	\$3E19	\$3E1A	\$3E1B	\$3E1C	\$3E1D
Com18	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25	\$3E26	\$3E27	\$3E28	\$3E29	\$3E2A	\$3E2B	\$3E2C	\$3E2D
Com19	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35	\$3E36	\$3E37	\$3E38	\$3E39	\$3E3A	\$3E3B	\$3E3C	\$3E3D
Com20	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45	\$3E46	\$3E47	\$3E48	\$3E49	\$3E4A	\$3E4B	\$3E4C	\$3E4D
Com21	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55	\$3E56	\$3E57	\$3E58	\$3E59	\$3E5A	\$3E5B	\$3E5C	\$3E5D
Com22	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65	\$3E66	\$3E67	\$3E68	\$3E69	\$3E6A	\$3E6B	\$3E6C	\$3E6D
Com23	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75	\$3E76	\$3E77	\$3E78	\$3E79	\$3E7A	\$3E7B	\$3E7C	\$3E7D
Com24	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85	\$3E86	\$3E87	\$3E88	\$3E89	\$3E8A	\$3E8B	\$3E8C	\$3E8D
Com25	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95	\$3E96	\$3E97	\$3E98	\$3E99	\$3E9A	\$3E9B	\$3E9C	\$3E9D
Com26	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5	\$3EA6	\$3EA7	\$3EA8	\$3EA9	\$3EAA	\$3EAB	\$3EAC	\$3EAD
Com27	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5	\$3EB6	\$3EB7	\$3EB8	\$3EB9	\$3EBA	\$3EBB	\$3EBC	\$3EBD
Com28	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5	\$3EC6	\$3EC7	\$3EC8	\$3EC9	\$3ECA	\$3ECB	\$3ECC	\$3ECD
Com29	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5	\$3ED6	\$3ED7	\$3ED8	\$3ED9	\$3EDA	\$3EDB	\$3EDC	\$3EDD
Com30	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5	\$3EE6	\$3EE7	\$3EE8	\$3EE9	\$3EEA	\$3EEB	\$3EEC	\$3EED
Com31	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5	\$3EF6	\$3EF7	\$3EF8	\$3EF9	\$3EFA	\$3EFB	\$3EFC	\$3EFD
Com32	\$3F00	\$3F01	\$3F02	\$3F03	\$3F04	\$3F05	\$3F06	\$3F07	\$3F08	\$3F09	\$3F0A	\$3F0B	\$3F0C	\$3F0D
Com33	\$3F10	\$3F11	\$3F12	\$3F13	\$3F14	\$3F15	\$3F16	\$3F17	\$3F18	\$3F19	\$3F1A	\$3F1B	\$3F1C	\$3F1D
Com34	\$3F20	\$3F21	\$3F22	\$3F23	\$3F24	\$3F25	\$3F26	\$3F27	\$3F28	\$3F29	\$3F2A	\$3F2B	\$3F2C	\$3F2D
Com35	\$3F30	\$3F31	\$3F32	\$3F33	\$3F34	\$3F35	\$3F36	\$3F37	\$3F38	\$3F39	\$3F3A	\$3F3B	\$3F3C	\$3F3D
Com36	\$3F40	\$3F41	\$3F42	\$3F43	\$3F44	\$3F45	\$3F46	\$3F47	\$3F48	\$3F49	\$3F4A	\$3F4B	\$3F4C	\$3F4D

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95	S96- S103	S104- S111
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7
Com37	\$3F50	\$3F51	\$3F52	\$3F53	\$3F54	\$3F55	\$3F56	\$3F57	\$3F58	\$3F59	\$3F5A	\$3F5B	\$3F5C	\$3F5D
Com38	\$3F60	\$3F61	\$3F62	\$3F63	\$3F64	\$3F65	\$3F66	\$3F67	\$3F68	\$3F69	\$3F6A	\$3F6B	\$3F6C	\$3F6D
Com39	\$3F70	\$3F71	\$3F72	\$3F73	\$3F74	\$3F75	\$3F76	\$3F77	\$3F78	\$3F79	\$3F7A	\$3F7B	\$3F7C	\$3F7D
Com40	\$3F80	\$3F81	\$3F82	\$3F83	\$3F84	\$3F85	\$3F86	\$3F87	\$3F88	\$3F89	\$3F8A	\$3F8B	\$3F8C	\$3F8D
Com41	\$3F90	\$3F91	\$3F92	\$3F93	\$3F94	\$3F95	\$3F96	\$3F97	\$3F98	\$3F99	\$3F9A	\$3F9B	\$3F9C	\$3F9D
Com42	\$3FA0	\$3FA1	\$3FA2	\$3FA3	\$3FA4	\$3FA5	\$3FA6	\$3FA7	\$3FA8	\$3FA9	\$3FAA	\$3FAB	\$3FAC	\$3FAD
Com43	\$3FB0	\$3FB1	\$3FB2	\$3FB3	\$3FB4	\$3FB5	\$3FB6	\$3FB7	\$3FB8	\$3FB9	\$3FBA	\$3FBB	\$3FBC	\$3FBD
Com44	\$3FC0	\$3FC1	\$3FC2	\$3FC3	\$3FC4	\$3FC5	\$3FC6	\$3FC7	\$3FC8	\$3FC9	\$3FCA	\$3FCB	\$3FCC	\$3FCD
Com45	\$3FD0	\$3FD1	\$3FD2	\$3FD3	\$3FD4	\$3FD5	\$3FD6	\$3FD7	\$3FD8	\$3FD9	\$3FDA	\$3FDB	\$3FDC	\$3FDD
Com46	\$3FE0	\$3FE1	\$3FE2	\$3FE3	\$3FE4	\$3FE5	\$3FE6	\$3FE7	\$3FE8	\$3FE9	\$3FEA	\$3FEB	\$3FEC	\$3FED
Com47	\$3FF0	\$3FF1	\$3FF2	\$3FF3	\$3FF4	\$3FF5	\$3FF6	\$3FF7	\$3FF8	\$3FF9	\$3FFA	\$3FFB	\$3FFC	\$3FFD

9.7. LCD Address Mapping for GPLB39: 32x112,16x112,8x112

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95	S96- S103	S104- S111
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7
Com0	\$3E00	\$3E01	\$3E02	\$3E03	\$3E04	\$3E05	\$3E06	\$3E07	\$3E08	\$3E09	\$3E0A	\$3E0B	\$3E0C	\$3E0D
Com1	\$3E10	\$3E11	\$3E12	\$3E13	\$3E14	\$3E15	\$3E16	\$3E17	\$3E18	\$3E19	\$3E1A	\$3E1B	\$3E1C	\$3E1D
Com2	\$3E20	\$3E21	\$3E22	\$3E23	\$3E24	\$3E25	\$3E26	\$3E27	\$3E28	\$3E29	\$3E2A	\$3E2B	\$3E2C	\$3E2D
Com3	\$3E30	\$3E31	\$3E32	\$3E33	\$3E34	\$3E35	\$3E36	\$3E37	\$3E38	\$3E39	\$3E3A	\$3E3B	\$3E3C	\$3E3D
Com4	\$3E40	\$3E41	\$3E42	\$3E43	\$3E44	\$3E45	\$3E46	\$3E47	\$3E48	\$3E49	\$3E4A	\$3E4B	\$3E4C	\$3E4D
Com5	\$3E50	\$3E51	\$3E52	\$3E53	\$3E54	\$3E55	\$3E56	\$3E57	\$3E58	\$3E59	\$3E5A	\$3E5B	\$3E5C	\$3E5D
Com6	\$3E60	\$3E61	\$3E62	\$3E63	\$3E64	\$3E65	\$3E66	\$3E67	\$3E68	\$3E69	\$3E6A	\$3E6B	\$3E6C	\$3E6D
Com7	\$3E70	\$3E71	\$3E72	\$3E73	\$3E74	\$3E75	\$3E76	\$3E77	\$3E78	\$3E79	\$3E7A	\$3E7B	\$3E7C	\$3E7D
Com8	\$3E80	\$3E81	\$3E82	\$3E83	\$3E84	\$3E85	\$3E86	\$3E87	\$3E88	\$3E89	\$3E8A	\$3E8B	\$3E8C	\$3E8D
Com9	\$3E90	\$3E91	\$3E92	\$3E93	\$3E94	\$3E95	\$3E96	\$3E97	\$3E98	\$3E99	\$3E9A	\$3E9B	\$3E9C	\$3E9D
Com10	\$3EA0	\$3EA1	\$3EA2	\$3EA3	\$3EA4	\$3EA5	\$3EA6	\$3EA7	\$3EA8	\$3EA9	\$3EAA	\$3EAB	\$3EAC	\$3EAD
Com11	\$3EB0	\$3EB1	\$3EB2	\$3EB3	\$3EB4	\$3EB5	\$3EB6	\$3EB7	\$3EB8	\$3EB9	\$3EBA	\$3EBB	\$3EBC	\$3EBD
Com12	\$3EC0	\$3EC1	\$3EC2	\$3EC3	\$3EC4	\$3EC5	\$3EC6	\$3EC7	\$3EC8	\$3EC9	\$3ECA	\$3ECB	\$3ECC	\$3ECD
Com13	\$3ED0	\$3ED1	\$3ED2	\$3ED3	\$3ED4	\$3ED5	\$3ED6	\$3ED7	\$3ED8	\$3ED9	\$3EDA	\$3EDB	\$3EDC	\$3EDD
Com14	\$3EE0	\$3EE1	\$3EE2	\$3EE3	\$3EE4	\$3EE5	\$3EE6	\$3EE7	\$3EE8	\$3EE9	\$3EEA	\$3EEB	\$3EEC	\$3EED
Com15	\$3EF0	\$3EF1	\$3EF2	\$3EF3	\$3EF4	\$3EF5	\$3EF6	\$3EF7	\$3EF8	\$3EF9	\$3EFA	\$3EFB	\$3EFC	\$3EFD
Com16	\$3F00	\$3F01	\$3F02	\$3F03	\$3F04	\$3F05	\$3F06	\$3F07	\$3F08	\$3F09	\$3F0A	\$3F0B	\$3F0C	\$3F0D
Com17	\$3F10	\$3F11	\$3F12	\$3F13	\$3F14	\$3F15	\$3F16	\$3F17	\$3F18	\$3F19	\$3F1A	\$3F1B	\$3F1C	\$3F1D
Com18	\$3F20	\$3F21	\$3F22	\$3F23	\$3F24	\$3F25	\$3F26	\$3F27	\$3F28	\$3F29	\$3F2A	\$3F2B	\$3F2C	\$3F2D
Com19	\$3F30	\$3F31	\$3F32	\$3F33	\$3F34	\$3F35	\$3F36	\$3F37	\$3F38	\$3F39	\$3F3A	\$3F3B	\$3F3C	\$3F3D
Com20	\$3F40	\$3F41	\$3F42	\$3F43	\$3F44	\$3F45	\$3F46	\$3F47	\$3F48	\$3F49	\$3F4A	\$3F4B	\$3F4C	\$3F4D
Com21	\$3F50	\$3F51	\$3F52	\$3F53	\$3F54	\$3F55	\$3F56	\$3F57	\$3F58	\$3F59	\$3F5A	\$3F5B	\$3F5C	\$3F5D
Com22	\$3F60	\$3F61	\$3F62	\$3F63	\$3F64	\$3F65	\$3F66	\$3F67	\$3F68	\$3F69	\$3F6A	\$3F6B	\$3F6C	\$3F6D

	S0- S7	S8- S15	S16- S23	S24- S31	S32- S39	S40- S47	S48- S55	S56- S63	S64- S71	S72- S79	S80- S87	S88- S95	S96- S103	S104- S111
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	B0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7
Com23	\$3F70	\$3F71	\$3F72	\$3F73	\$3F74	\$3F75	\$3F76	\$3F77	\$3F78	\$3F79	\$3F7A	\$3F7B	\$3F7C	\$3F7D
Com24	\$3F80	\$3F81	\$3F82	\$3F83	\$3F84	\$3F85	\$3F86	\$3F87	\$3F88	\$3F89	\$3F8A	\$3F8B	\$3F8C	\$3F8D
Com25	\$3F90	\$3F91	\$3F92	\$3F93	\$3F94	\$3F95	\$3F96	\$3F97	\$3F98	\$3F99	\$3F9A	\$3F9B	\$3F9C	\$3F9D
Com26	\$3FA0	\$3FA1	\$3FA2	\$3FA3	\$3FA4	\$3FA5	\$3FA6	\$3FA7	\$3FA8	\$3FA9	\$3FAA	\$3FAB	\$3FAC	\$3FAD
Com27	\$3FB0	\$3FB1	\$3FB2	\$3FB3	\$3FB4	\$3FB5	\$3FB6	\$3FB7	\$3FB8	\$3FB9	\$3FBA	\$3FBB	\$3FBC	\$3FBD
Com28	\$3FC0	\$3FC1	\$3FC2	\$3FC3	\$3FC4	\$3FC5	\$3FC6	\$3FC7	\$3FC8	\$3FC9	\$3FCA	\$3FCB	\$3FCC	\$3FCD
Com29	\$3FD0	\$3FD1	\$3FD2	\$3FD3	\$3FD4	\$3FD5	\$3FD6	\$3FD7	\$3FD8	\$3FD9	\$3FDA	\$3FDB	\$3FDC	\$3FDD
Com30	\$3FE0	\$3FE1	\$3FE2	\$3FE3	\$3FE4	\$3FE5	\$3FE6	\$3FE7	\$3FE8	\$3FE9	\$3FEA	\$3FEB	\$3FEC	\$3FED
Com31	\$3FF0	\$3FF1	\$3FF2	\$3FF3	\$3FF4	\$3FF5	\$3FF6	\$3FF7	\$3FF8	\$3FF9	\$3FFA	\$3FFB	\$3FFC	\$3FFD

Note:

LCD Address Mapping (CPU Side) for GPLB39A/GPLB39B.

Duty 1/64 (\$3C00~3FFF)

Duty 1/48 (\$3D00~3FFF)

Duty 1/32 (\$3E00~3FFF)

Duty 1/16 (\$3E00~3EFF)

Duty 1/8 (\$3E00~3E7F)

10. LCD Driver

10.1. LCD Driver Feature Table for GPLB3X

	LB30EV Chip *LB30B EV Chip	GPLB30/33A	GPLB31/32/37	GPLB33B
Vlcd	2.45V ~ 5.75V 2.95V ~ 6.85V	2.45V ~ 5.75V	2.45V ~ 5.75V 2.95V ~ 6.85V	2.98-5.75V
Bias	1/3*, 1/4*, 1/5, 1/6	1/5	1/5, 1/6	1/3*, 1/4*, 1/5
Duty	1/4*, 1/8*, 1/16, 1/32	1/16	1/16, 1/32	1/4*, 1/8*, 1/16
Frame Rate	64Hz/68Hz* 73Hz*/79Hz*	64Hz	64Hz	64Hz/68Hz* 73Hz*/79Hz*

LB30 EV Chip : GPLB30EMU Board V1.4 or earlier versions.

LB30B EV Chip : GPLB30EMU Board V2.1 or later versions.

	LB35EV Chip	GPLB34	GPLB35/36
Vlcd	2.45V ~ 5.75V 2.95V ~ 6.85V 3.53V ~ 8.21V	2.45V ~ 5.75V	2.45V ~ 5.75V 2.95V ~ 6.85V 3.53V ~ 8.21V
Bias	1/5, 1/6, 1/7, 1/8	1/5, 1/6	1/5, 1/6, 1/7, 1/8
Duty	1/16, 1/32, 1/36, 1/48	1/16	1/16, 1/32, 1/36, 1/48
Frame Rate	56.8HZ/64Hz	64Hz	56.8HZ/64Hz

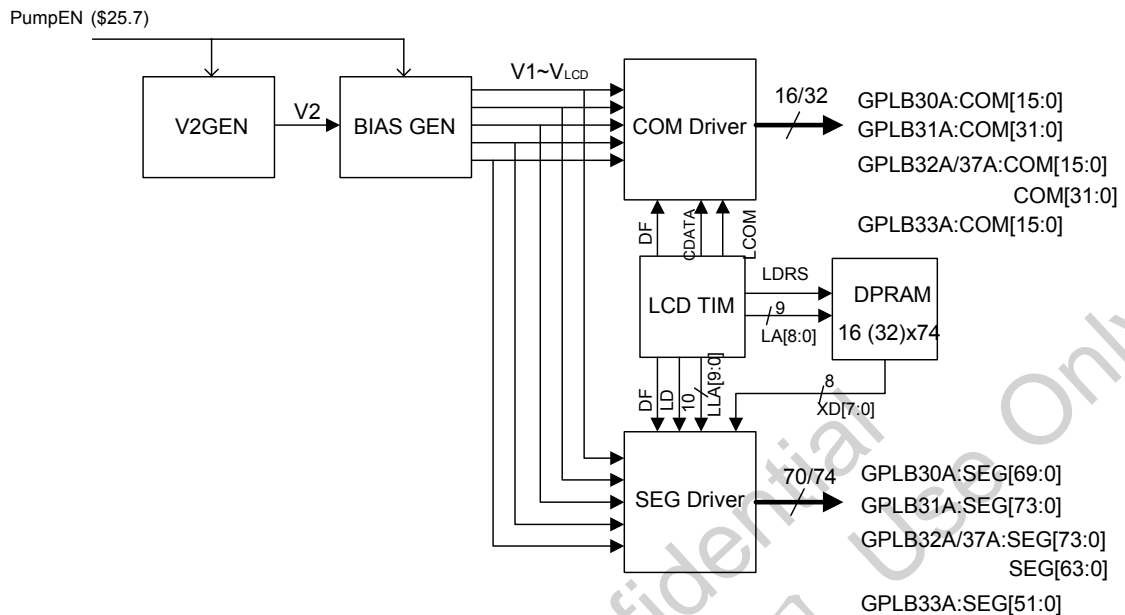
56.8Hz: 1/48 duty , other duty LCD frame rate = 64Hz

	LB39EV Chip	GPLB39A	GPLB39B
Vlcd	4.4V ~ 5.7V 5.28V~6.83V 6.2V~8.06V	2.45V ~ 5.75V 2.95V~6.85V 3.53V~8.21V	4.4V ~ 5.7V 5.28V~6.83V 6.2V~8.06V
Bias	1/4, 1/5, 1/6, 1/7, 1/8, 1/9	1/4, 1/5, 1/6, 1/7, 1/8, 1/9	1/4, 1/5, 1/6, 1/7, 1/8, 1/9
Duty	1/8, 1/16, 1/32, 1/48, 1/64	1/8, 1/16, 1/32, 1/48, 1/64	1/8, 1/16, 1/32, 1/48, 1/64
Frame Rate	62Hz/64Hz	62Hz/64Hz	62Hz/64Hz

62Hz: 1/48 duty , other duty LCD frame rate = 64Hz

Note: The Vlcd, bias and duty are software programmable.

10.2. GPLB30/31/32/33A/37 LCD Driver Block Diagram



* If PumpEN(\$25.7)=0, then V1 ~ V4=0, V_{LCD}=VDD. LCD is unable to display normally.

10.3. Function Description

The LCD driver consists of six major sub-modules:

– V2GEN

This sub-module generates a reference voltage V2 for BIAS_GEN to generate the LCD bias voltages.

– BIAS_GEN

The BIAS_GEN sub-module is a 2.5x-3.0X (1/5-1/6 bias) charge-pumping circuit. This sub-module generates other LCD bias voltages (V1, V3-V4, VLCD) through charge-pump.

– LCD_TIM

This sub-module generates all the necessary timing signals for COM driver, SEG driver and DPRAM.

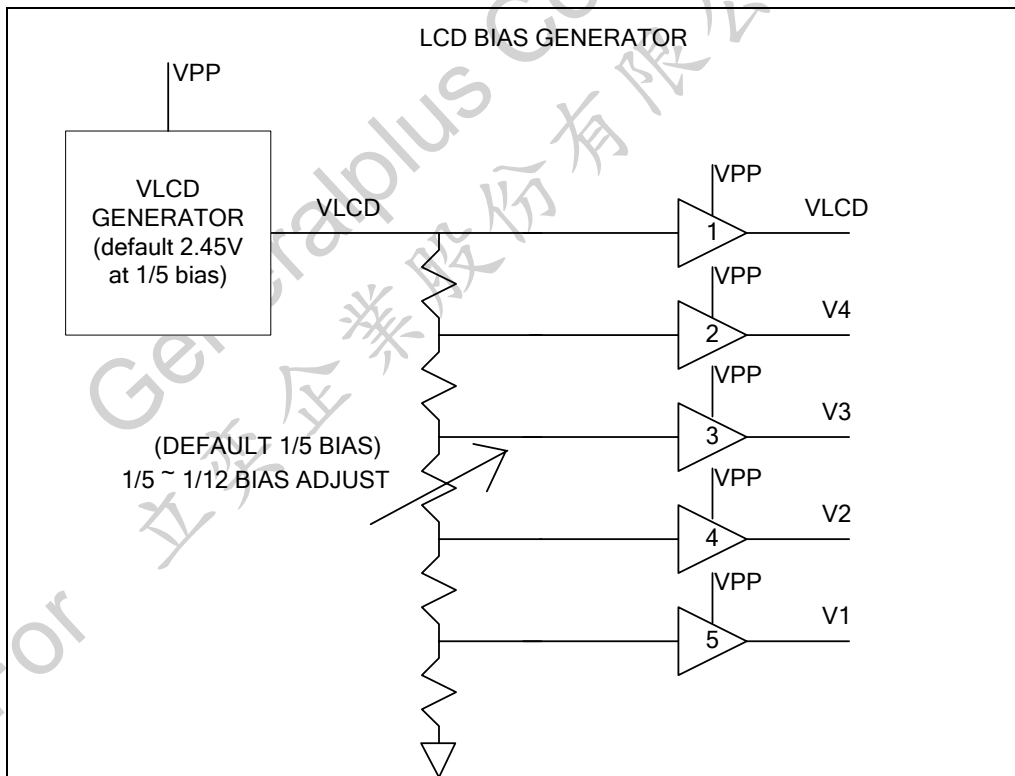
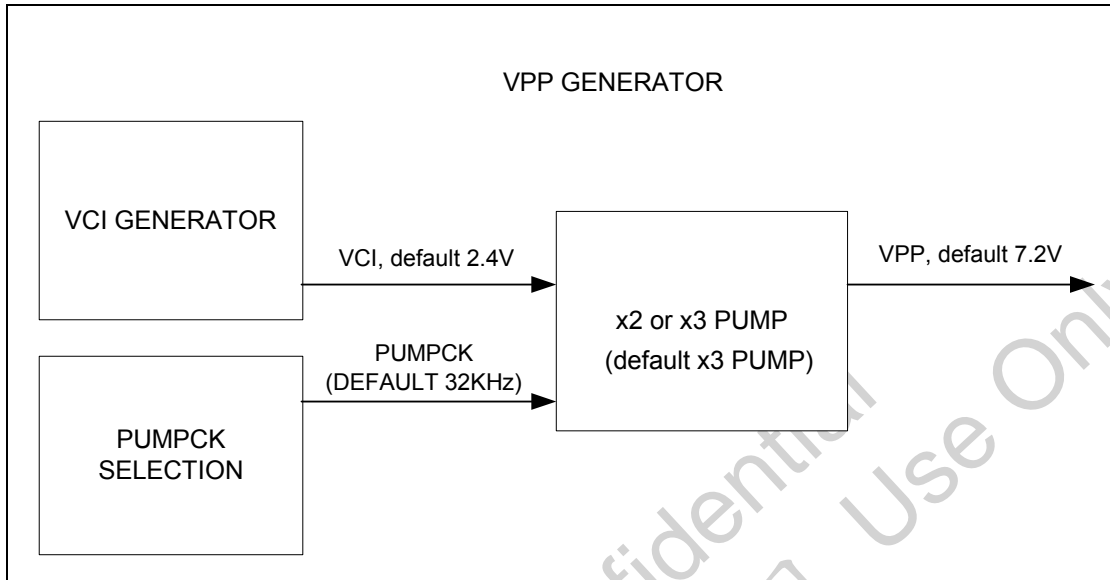
1) COM Driver

The COM driver sub-module generates the LCD common scan waveforms sequentially.

2) SEG Driver

The SEG driver sub-module generates the LCD segment waveforms according to the contents of LCD buffer RAM (DPRAM).

10.4. GPLB34/35/36/39 LCD Driver Block Diagram

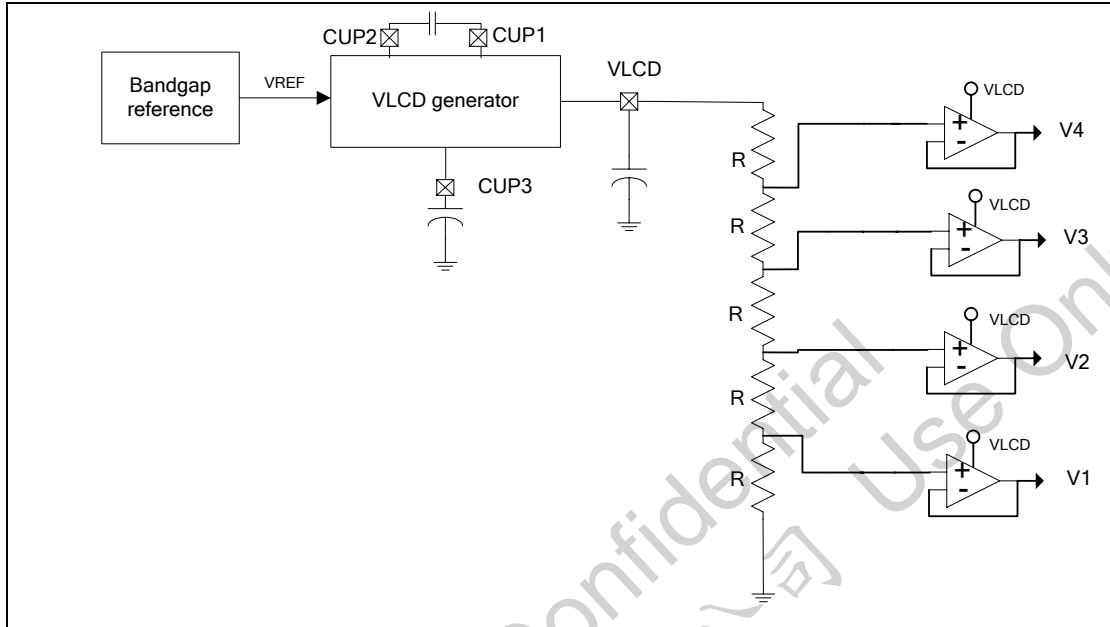


Note:

1. VPP will drop 0.4V as VPP supply 100uA current. The condition is 2KHz pumping clock, 1uF capacitor.
2. If PumpEN(\$25.7)=0, then V1 ~ V4=0, VLCD=VDD. LCD is unable to display normally.

10.5. GPLB33B LCD Driver Block Diagram

LCD driver reference



LCD Control Register Address Mapping

NAME	ADDRESS	R/W	b7	b6	b5	b4	b3	b2	b1	b0
LCDOPT	\$24	R/W	DUTYB7	DUTYB6	BOP1	BOP0	ALL_OFF	ALL_ON	STRBEN	LCDEN
PUMPCTL	\$25	R/W	PUMPEN	-	-	-	-	-	PUMP1	PUMP0
VLCDCTL	\$26	R/W	-	-	-	E4	E3	E2	E1	E0
LCDCTL1	\$2E	R/W	Duty1	Duty0	Bias2	VCIB2	VCIB1	VCIB0	Bias1	Bias0

10.6. P_24H_LCD_Option_Setting (\$24) (W)

P_LCD_Option_Setting			0x24		LCD Option Control				
Bit	7	6	5	4	3	2	1	0	
Function	DUTYB7	DUTYB6	BOP1	BOP0	ALL_OFF	ALL_ON	STRBEN	LCDEN	
Default	0	0	0	0	0	0	0	0	

Bit	Function	Type	Description	Condition
7:6	DUTY	R/W	Set LCD Duty(GPLB30/31/32/33/37); Read LCD Duty	GPLB33B X:0 = 1/16 duty (default) 1:1 = 1/8 duty 0:1 = 1/4 duty GPLB30/GPLB33A X:0= 1/16 (default) X:1= N/A

Bit	Function	Type	Description	Condition
				GPLB31/32/37 X:0 = 1/16 (default) X:1 = 1/32
5 : 4	BOP	R/W	Set LCD Bias(GPLB30/31/32/33/37); Read LCD Bias	GPLB33B 0:X = 1/5 bias (default) 1:1 = 1/4 bias 1:0 = 1/3 bias GPLB30/GPLB33A 0:0= 1/5 bias (default) 0:1= N/A 1:X= N/A GPLB31/32/37 00= 1/5 bias (default) 01= 1/6 bias 1X= N/A
3	ALL_OFF	W	LCD display normal operation or all off.regardless of LCD ram contents.	0= Normal Operation 1= LCD display all off
		R	Read LCD display status	
2	ALL_ON	W	LCD display normal operation or all on regardless of LCD ram contents. If ALL_OFF and ALL_ON are both set to "1", ALL_ON is activated. Moreover, setting ALL_OFF and ALL_ON does not interfere with LCD RAM.	0= Normal Operation 1= LCD display all on
		R	Read LCD display status	
1	STRBEN	W	Enable/Disable LCD strobe waveform output In key scan routine, this bit must be "0". (Disable LCD strobe waveform)	0= disable 1= enable
		R	Read LCD strobe status	
0	LCDEN	W	LCD enable/disable	0= LCD disable 1= LCD enable
		R	Read LCD status	

10.7. P_25H_LCD_Pump_Control (\$25) (W)

P_LCD_Pump_Control			0x25		LCD Charge Pump Control			
Bit	7	6	5	4	3	2	1	0
Function	PUMPEN	-	-	-	DIV1	DIV0	PUMP1	PMP0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	PUMPEN	W	Enable/Disable LCD charge pump 1. It must be disabled before entering standby mode to save	0= disable 1= enable

Bit	Function	Type	Description	Condition
			power. 2. PUMPEN must be enabled to display LCD. 3. When PumpEN is enabled (=1), V _{LCD} must be set larger than V _{dd} . Otherwise, extra current consumption will occur	
		R	Read LCD charge pump status	
3:2	DIV	W	Set LCD frame rate(only for GPLB33B)	GPLB33B: 00=64Hz
3:2	DIV	R	Read LCD frame rate(only for GPLB33B)	01=68Hz 10=73Hz 11=79Hz
1 : 0	PUMP clock	W	Set LCD charge pump clock	00= 32kHz 01= 16kHz
		R	Read LCD charge pump clock	10= 8kHz 11= 4kHz

10.8. P_26H_VLCD_Voltage_Control (\$26) (R/W)

P_VLCD_Voltage_Control		0x26				VLCD Voltage Control			
Bit	7	6	5	4	3	2	1	0	
Function	-	-	-	-	VLCD SEL				
Default	0	0	0	0	0	0	0	0	

Bit	Function	Type	Description	Condition
4 : 0	VLCD SEL	W	VLCD voltage selection ,VLCD must higher then VDD	See below table
		R	Read VLCD voltage	

VLCD=2.45V~5.75V, 32-level (1/4 bias, 1/5 bias)

2.95V~6.85V, 32-level (1/6, 1/7 bias)

3.53V~8.21V, 32-level (1/8 bias,1/9 bias)

*(This table not include GPLB39B)

\$26.4 ~ \$26.0					1/5 bias	1/6, 1/7 bias	1/8,1/9 bias
b4	b3	b2	b1	b0	2.45 + (A*0.1064)	2.95 + (A*0.1258)	3.53+(A*0.151)
0	0	0	0	0	2.45*	2.95	3.53
0	0	0	0	1	2.56*	3.08	3.67
0	0	0	1	0	2.66*	3.20	3.83
0	0	0	1	1	2.77*	3.33	3.97
0	0	1	0	0	2.88*	3.45	4.12

\$26.4 ~ \$26.0					1/5 bias 2.45 + (A*0.1064)	1/6, 1/7 bias 2.95 + (A*0.1258)	1/8,1/9 bias 3.53+(A*0.151)
b4	b3	b2	b1	b0			
0	0	1	0	1	2.98	3.58	4.25
0	0	1	1	0	3.09	3.71	4.43
0	0	1	1	1	3.19	3.83	4.56
0	1	0	0	0	3.30	3.96	4.71
0	1	0	0	1	3.41	4.08	4.86
0	1	0	1	0	3.51	4.21	5.03
0	1	0	1	1	3.62	4.33	5.18
0	1	1	0	0	3.73	4.46	5.33
0	1	1	0	1	3.83	4.59	5.47
0	1	1	1	0	3.94	4.71	5.63
0	1	1	1	1	4.05	4.84	5.77
1	0	0	0	0	4.15	4.96	5.92
1	0	0	0	1	4.26	5.09	6.08
1	0	0	1	0	4.37	5.21	6.23
1	0	0	1	1	4.47	5.34	6.38
1	0	1	0	0	4.58	5.47	6.54
1	0	1	0	1	4.68	5.59	6.68
1	0	1	1	0	4.79	5.72	6.81
1	0	1	1	1	4.90	5.84	6.98
1	1	0	0	0	5.00	5.97	7.13
1	1	0	0	1	5.11	6.10	7.29
1	1	0	1	0	5.22	6.22	7.43
1	1	0	1	1	5.32	6.35	7.6
1	1	1	0	0	5.43	6.47	7.75
1	1	1	0	1	5.54	6.60	7.91
1	1	1	1	0	5.64	6.72	8.05
1	1	1	1	1	5.75	6.85	8.21

* : Not available in GPLB33B

The following table is only for GPLB39B

VLCD= 4.4V~5.702V, 32-level (1/4 bias, 1/5 bias)

5.28V~6.83V, 32-level (1/6, 1/7 bias)

6.2V~8.06V, 32-level (1/8 bias,1/9 bias)

\$26.4 ~ \$26.0					1/5 bias	1/6, 1/7 bias	1/8,1/9 bias
b4	b3	b2	b1	b0	2.45 + (A*0.1064)	2.95 + (A*0.1258)	6.2+(A*0.06)
0	0	0	0	0	4.400	5.28	6.20
0	0	0	0	1	4.442	5.33	6.26

\$26.4 ~ \$26.0					1/5 bias	1/6, 1/7 bias	1/8,1/9 bias
b4	b3	b2	b1	b0	2.45 + (A*0.1064)	2.95 + (A*0.1258)	6.2+(A*0.06)
0	0	0	1	0	4.484	5.38	6.32
0	0	0	1	1	4.526	5.43	6.38
0	0	1	0	0	4.568	5.48	6.44
0	0	1	0	1	4.610	5.53	6.50
0	0	1	1	0	4.652	5.58	6.56
0	0	1	1	1	4.694	5.63	6.62
0	1	0	0	0	4.736	5.68	6.68
0	1	0	0	1	4.778	5.73	6.74
0	1	0	1	0	4.820	5.78	6.80
0	1	0	1	1	4.862	5.83	6.86
0	1	1	0	0	4.904	5.88	6.92
0	1	1	0	1	4.946	5.93	6.98
0	1	1	1	0	4.988	5.98	7.04
0	1	1	1	1	5.030	6.03	7.10
1	0	0	0	0	5.072	6.08	7.16
1	0	0	0	1	5.114	6.13	7.22
1	0	0	1	0	5.156	6.18	7.28
1	0	0	1	1	5.198	6.23	7.34
1	0	1	0	0	5.240	6.28	7.40
1	0	1	0	1	5.282	6.33	7.46
1	0	1	1	0	5.324	6.38	7.52
1	0	1	1	1	5.366	6.43	7.58
1	1	0	0	0	5.408	6.48	7.64
1	1	0	0	1	5.450	6.53	7.70
1	1	0	1	0	5.492	6.58	7.76
1	1	0	1	1	5.534	6.63	7.82
1	1	1	0	0	5.576	6.68	7.88
1	1	1	0	1	5.618	6.73	7.94
1	1	1	1	0	5.660	6.78	8.00
1	1	1	1	1	5.702	6.83	8.06

*All calculated figures above are typical values.

Note:

1. The tolerances for above figures are all $\pm 5\%$.
2. GPLB35/36 has no limitation on bias vs. VLCD. So, it can have 96-level contrast adjustment.

10.9. P_2EH_LCD_CTL1 (\$002E) (R/W)

P_LCD_CTL1			0x2E		LCD Bias/Duty/Voltage Control			
Bit	7	6	5	4	3	2	1	0
Function	Duty1	Duty0	Bias2	VCIB2	VCIB1	VCIB0	Bias1	Bias0
Default	0	0	x/0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 6	DUTY	W	Set the LCD Duty	See below description
		R	Read LCD Duty	
5 : 1 : 0	Bias	W	Set the LCD Bias	See below description
		R	Read LCD Bias	
4 : 2	VCI voltage	W	Set the VCI voltage	See below description
		R	Read VCI voltage	

GPLB34/35/36 (b7,b6) : Duty option
 : (0,0): 1/16 duty (default)
 : (0,1): 1/32 duty
 : (1,0): 1/36 duty(GPLB34 N/A)
 : (1,1): 1/48 duty(GPLB34 N/A)

GPLB34/35/36 (b5, b1,b0) : Bias option
 : (x, 0,0): 1/5 bias (default)
 : (x, 0,1): 1/6 bias
 : (x, 1,0): 1/7 bias(GPLB34 N/A)
 : (x, 1,1): 1/8 bias(GPLB34 N/A)

GPLB39 (b7,b6) : Duty option
 : (0,0): 1/16 duty (default)
 : (0,1): 1/32 duty
 : (1,0): 1/8 duty
 : (1,1): 1/48 duty

GPLB39 (b5, b1,b0) : Bias option
 : (0, 0,0): 1/5 bias (default)
 : (0, 0,1): 1/6 bias
 : (0, 1,0): 1/7 bias
 : (0, 1,1): 1/8 bias
 : (1, 0,0): 1/4 bias
 : (1, 1,1): 1/9 bias
 : (1, 0,1): 1/9 bias
 : (1, 1,0): 1/9 bias

Note:

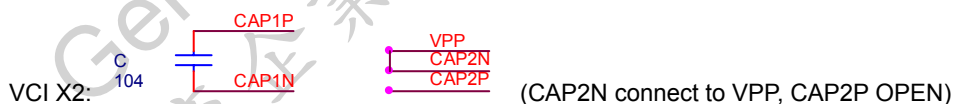
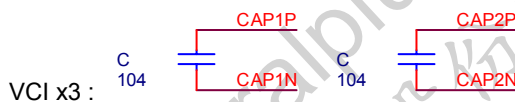
1. This register is only available in GPLB34/35/36/39.
2. GPLB34/35/36 Body: When duty is set to 1/16 duty, the COMMON is auto-configured to 16-common as well. Similarly, if duty is set to 1/32 duty, a 32-common is selected. Same criteria are applies to other duties. As a result, five LCD configurations are available in GPLB35/36, 16*74, 32*74, 32*100, 36*96 and 48*84.
3. GPLB39: Five LCD configurations are available in GPLB39, 8*112, 16*112, 32*112 , 48*112, 64*96. And LCD matrix 64*96 can be selected by P_3032H_LCD_CTL2.

(b4,b3,b2) <=> (VCIB2, VCIB1, VCIB0) :

VCIB2	VCIB1	VCIB0	VCI voltage	VCI x 2	VCI x 3
0	0	1	2.3V	VPP=4.6V	VPP=6.9V
0	0	0	2.4V	VPP=4.8V	VPP=7.2V
0	1	1	2.5V	VPP=5.0V	VPP=7.5V
0	1	0	2.7V	VPP=5.4V	VPP=8.1V
1	0	1	2.9V	VPP=5.8V	VPP=8.7V
1	0	0	3.5V	VPP=7.0V	VPP=10.5V
1	1	1	3.7V	VPP=7.4V	VPP=11.1V
1	1	0	Not Available		

Note:

1. The (VCIB2, VCIB1, VCIB0) in the table is not in ordinary numerical sequence. Cares must be exercised while configuring the VCI voltage.
2. In GPLB34/35/36/39, VPP can select VCI X2 or VCI X 3 by hardware setting.



3. Enable Charge pump (\$25.b7=1) will also enable the regulator which outputs VCI.
4. The VCI voltage can be supplied by external power source which cannot be lower than the internal VCI voltage.
5. In GPLB34/35/36/39 , (VPP – VLCD) must greater then 0.5V. If VDD < VCI , VCI , VLCD, VPP will be pulled down.

10.10. P_3032H_LCD_CTL2 (\$3032) (R/W)

P_LCD_CTL2			0x3032		COM/SEG Selection(GPLB35/36/39)			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
3 : 0	COM X SEG	W	Set the LCD COM X SEG	See below table
		R	Read LCD COM X SEG	

Note:

- This register is only available in GPLB35/36/39.
- GPLB35/36 Body: In 32-common mode, two LCD matrixes can be optioned: 32 (COM) x 74 (SEG) and 32 (COM) x100 (SEG). When 74-SEG is selected, set all b3 ~ b0 to "0". When 100-SEG is selected, set b3 ~ b0 to "1". No other setting can be given to b3 ~ b0.
- GPLB39 Body : 64 x 96 DOTS , \$3032 [b3 : b0] = 1111

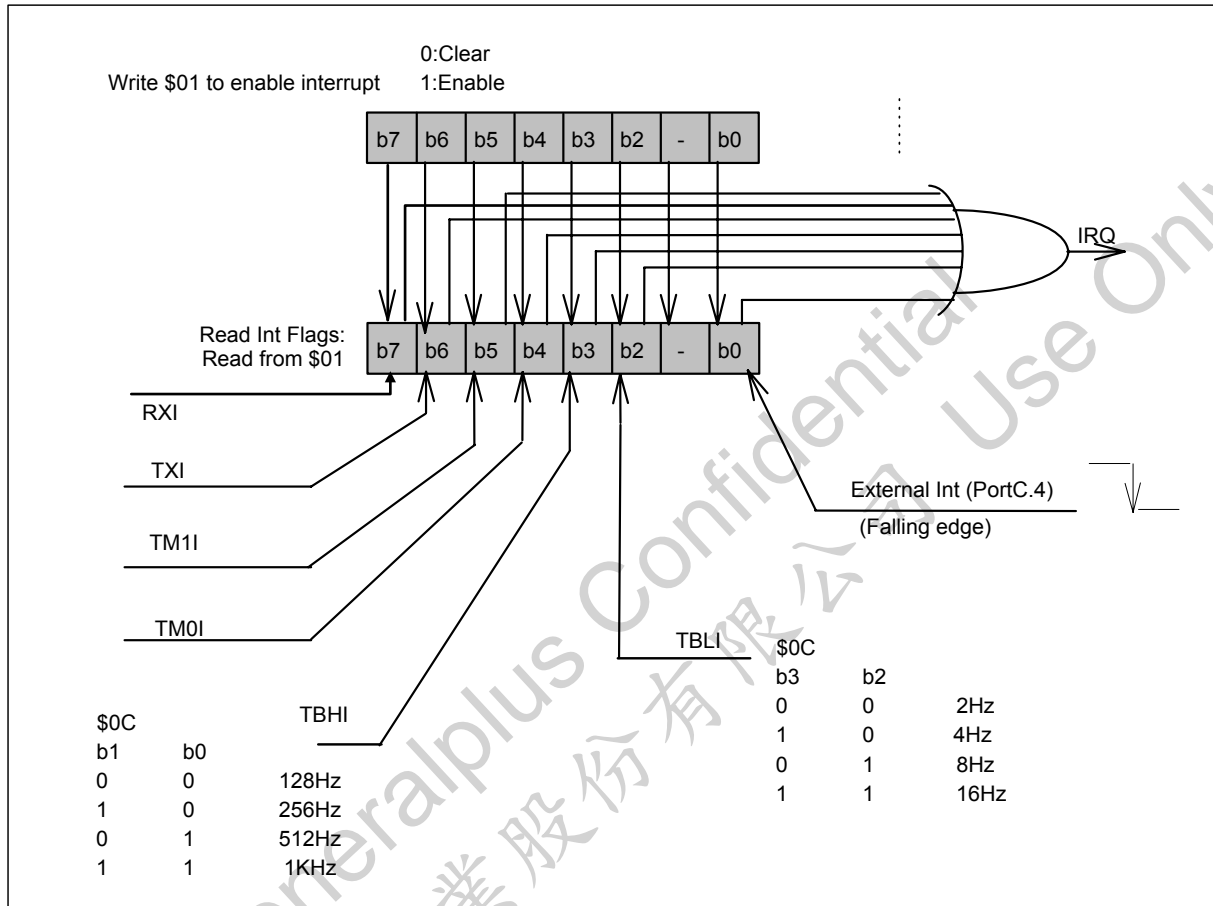
GPLB35/36

COM X SEG	b3 ~ b0
32 X 74	0000
32 X 100	1111
36 X 96	0000
48 X 48	0000

GPLB39

COM X SEG	b3 ~ b0
64 X 96(GPLB39)	1111
Other	0000

11. Interrupt /NMI



The following abbreviations are used for interrupt:

- RXI/RXIE/RXIC : UART receiver interrupt
- TXI/TXIE/TXIC : UART transmitter interrupt
- TM1I/TM1IE/TM1IC : Timer 1 interrupt
- TM0I/TM0IE/TM0IC : Timer 0 interrupt
- TBHI/TBHIIE/TBHIIC : Timer base 128/256/512/1kHz interrupt
- TBLI/TBLIE/TBLIC : Timer base 2/4/8/16Hz interrupt
- EXI/EXIE/EXIC : External interrupt (from PortC.4)

11.1. P_01H_Interrupt_Ctrl (\$01) (R/W)

P_Interrupt_Ctrl		0x01				Interrupt Selection		
Bit	7	6	5	4	3	2	1	0
Function	RX_IE	TX_IE	TM1_IE	TM0_IE	TBH_IE	TBL_IE	-	EX_IE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RX_IE	W	Set Rx Interrupt	0= disable/clear
		R	Read Rx Interrupt status	1= enable
6	TX_IE	W	Set Tx Interrupt	0= disable/clear
		R	Read Tx Interrupt status	1= enable
5	TM1_IE	W	Set Timer1 Interrupt	0= disable/clear
		R	Read Timer1 Interrupt status	1= enable
4	TM0_IE	W	Set Timer0 Interrupt	0= disable/clear
		R	Read Timer0 Interrupt status	1= enable
3	TBH_IE	W	Set TBH(128/256/512/1KHz) Interrupt	0= disable/clear
		R	Read TBH(128/256/512/1KHz) Interrupt status	1= enable
2	TBL_IE	W	Set TBL(2/4/8/16Hz)Interrupt	0= disable/clear
		R	Read TBL(2/4/8/16Hz)Interrupt status	1= enable
0	EX_IE	W	Set External Interrupt	0= disable/clear
		R	Read External Interrupt status	1= enable

Writing '1' to the corresponding bit enables its interrupt and reading the corresponding bit checks the interrupt status. Writing '0' to the corresponding bit to disable its interrupt and interrupt status flag will be cleared.

11.2. P_02H_Interrupt_Clear (\$02) (R/W)

P_Interrupt_Clar		0x02				Interrupt Clear		
Bit	7	6	5	4	3	2	1	0
Function	RX_IC	TX_IC	TM1_IC	TM0_IC	TBH_IC	TBL_IC	-	EX_IC
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RX_IC	W	Clear Rx Interrupt flag	1= clear
6	TX_IC	W	Clear Tx Interrupt flag	1= clear
5	TM1_IC	W	Clear Timer1 Interrupt flag	1= clear
4	TM0_IC	W	Clear Timer0 Interrupt flag	1= clear
3	TBH_IC	W	Clear TBH(128/256/512/1KHz) Interrupt flag	1= clear

Bit	Function	Type	Description	Condition
2	TBL_IC	W	Clear TBL(2/4/8/16Hz)Interrupt flag	1= clear
7	EX_IC	W	Clear External Interrupt flag	1= clear

Writing "1" to the corresponding bit clears interrupt flag. After an interrupt flag is read and determined, we recommend clearing the interrupt flag immediately.

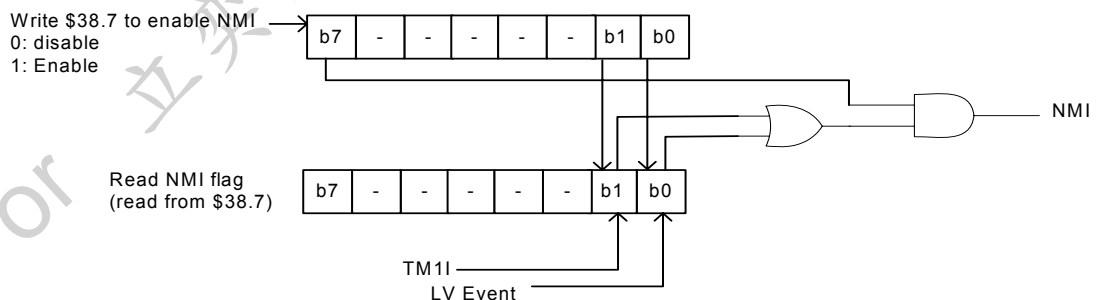
11.3. P_38H_NMI_Ctrl (R/W) (\$38) (Default: 00000000)

P_NMI_Ctrl			0x38		NMI Control			
Bit	7	6	5	4	3	2	1	0
Function	NMIEN	-	-	-	-	-	TM1 E	LV_E
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	NMIEN	W	Enable/Disable NMI	0= disable
		R	Read NMI status	1= enable
6	TM1_E	W	Timer1 NMI enable or disable	0= disable
		R	Read Timer1 NMI flag status	1= enable
5	LV_E	W	Low voltage NMI enable or disable	0= disable
		R	Read Low voltage NMI flag status	1= enable

Enable or disable NMI events including Timer1 NMI, and Low Voltage NMI. To enable TM1_E and LV_E, the NMIEN must be enabled.

NMI Structure



11.4. Interrupt Program Example

The sample program intends to enable RX, TX and 2Hz interrupts.

```

                                L_CheckTXInt:
LDA    #%00000000                LDA    R_IRQTemp
STA    P_0CH_TimeBaseSelect      AND    #%01000000
LDA    #%11000100                BEQ    L_CheckTBL
STA    P_01H_InterruptCtrl
STA    R_Int flags
:
:
Irq:
PHA
TXA
PHA
TYA
PHA
LDA    P_01H_InterruptCtrl
STA    P_02H_InterruptClear

                                L_TXIntRoutine:
:
:
L_CheckTBL:
LDA    R_IRQTemp
AND    #%00000100
BEQ    L_IRQEND
L_TBLRoutine:
:
:
L_IRQEND:
STA    R_IRQTemp                PLA
AND    #%10000000              TAY
BEQ    L_CheckTXInt            PLA
                                PLA
L_RXIntRoutine:                TAX
:                                PLA
:                                RTI

```

12. Sleep/Wakeup

The sleep mode (power-down) mode is a mode which the device is placed in its lowest current consumption state. The device oscillator is turned off and therefore, no system clocks are occurring in device. Sleep mode is entered by writing "07H" to CPU_Clock_Ctrl (\$04h). In such mode, if a wake-up source (event) is triggered, CPU awakens and continues to execute the rest of program.

Note: After turning off the strobe function, an interval period of at least 8 CPU clocks must be given to assure the PortA status is completely stabilized. Moreover, the wakeup source must be enabled before latching PortA. The procedure summary is as follows:

1. Enable wakeup sources.
2. Turn off key strobe function.
3. Interval period of at least 8 CPU clock cycles.
4. Latch PortA.
5. Stop clock to enter sleep mode.

For correct programming sequence, see the sleep examples below.

12.1. P_18H_Wakeup_Ctrl (\$18) (R/W)

The device can be awakened from standby and halt modes through one of the following events. Writing '1' to the corresponding bit enables its wakeup source and reading the corresponding bit checks the wakeup status. Writing '0' to the corresponding bit disables its wakeup and clears its wakeup flag.

P_Wakeup_Ctrl		0x18			Interrupt Selection			
Bit	7	6	5	4	3	2	1	0
Function	-	-	RXEN	TM1EN	TBHEN	TM0EN	TBLEN	KEYEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
5	RXEN	W	UART Rx signal wake-up	0= disable/clear
	RXW	R	Read Rx wake-up status	1= enable
4	TM1EN	W	Timer1 overflow wake-up	0= disable/clear
	TM1W	R	Read Timer1 wake-up status	1= enable
3	TBHEN	W	Time Base High wake-up	0= disable/clear
	TBHW	R	Read Time Base High wake-up status	1= enable
2	TM0EN	W	Timer0 overflow wake-up	0= disable/clear
	TM0W	R	Read Timer0 wake-up status	1= enable
1	TBLEN	W	Time Base Low wake-up	0= disable/clear
	TBLW	R	Read Time Base Low wake-up status	1= enable

Bit	Function	Type	Description	Condition
0	KEYEN	W	PortA key wake-up	0= disable/clear
	KEYW	R	Read PortA key wake-up status	1= enable

Note:

1. Make sure all wakeup status (R) flags are cleared and re-set the wakeup sources before entering into sleep mode. If not, the CPU may not wake up after sleep.
2. When wake up sources are TBLEN and KEYEN, it is very important to check if PortA strobe is disabled before clearing wakeup status and enabling wakeup source. If PortA strobe is disabled after clearing wakeup status and then enabling wakeup source, it may not enter into sleep. The Sleep process must be followed as bellow.

12.2. Sleep Program

```

;=====
; Sleep Procedure
; Programming to turn into 'Halt Mode' (LCD Display, but CPU stop)
;=====
Step 1: Disable PortA strobe function
LDA    #0
STA    P_05H_PortAStrobePull    ; disable PortA strobe before read PortA data
%WaitPortAReady                ; at least 8 CPU clock cycles delay to ensure PortA status
                                ; is ready
%TurnOnLCDstrobe                ; if using H/W Key scan function
Step 2: Enable wake up source
LDA    #0                        ; Clear wakeup status
STA    P_18H_WakeUpCtrl
LDA    #%00000011                ; Enable wakeup source
STA    P_18H_WakeUpCtrl          ; Suppose TBLEN and KEYEN is enabled

Step 3: Latch PortA data
LDA    P_08H_PortAData

Step 4: Stop CPU clock
LDA    #07H
STA    P_04H_CPUClkCtrl
NOP
NOP
NOP

;=====
; Programming to turn into "standby mode" (whole system OFF)
; Ex: Using PortA.0 as key wakeup source
; The recommended procedures are as follows:
;=====
Step 1: Key debounce before entering standby mode

```

Step 2: Clear LCD mapping RAM

```
JSR    ClearAllLcd
```

Step 3: Set ProtA.0 as key wakeup source

```
LDA    #0
STA    P_07H_ProtADir        ;set ProtA.0 input pull low
STA    P_06H_PortAConfig
STA    P_08H_PortAData
STA    P_05H_PortAStrobePH   ;set PortA as normal input I/O
```

Step 4: Turn off LCD, 32768Hz OSC

```
LDA    #0
STA    P_24H_LCDOPT         ; disable LCD(avoid a remained image)
STA    P_25H_LCD_pump_control ; disable LCD pump function (avoid current consumption)
STA    P_0E_C32KCtrl        ; disable 32768Hz OSC
```

Step 5: Enable wakeup source

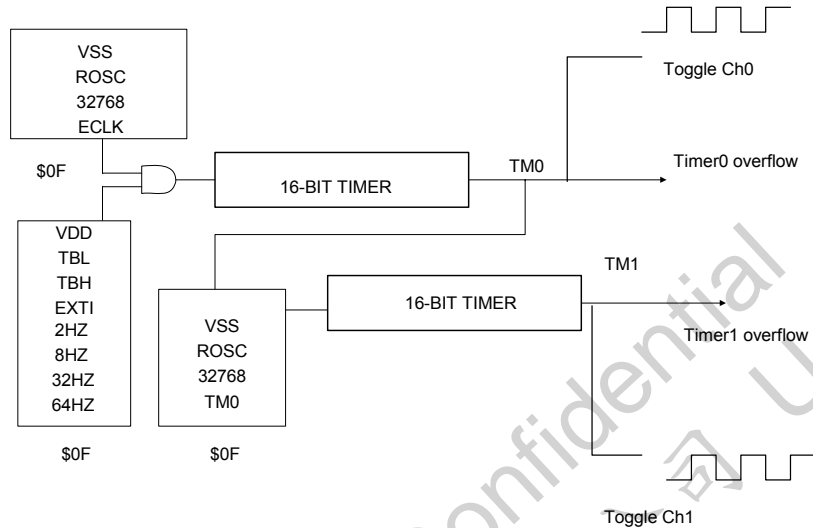
```
LDA    #0                    ; clear wakeup source
STA    P_18H_WakeUpCtrl
LDA    #%00000001           ; enable KEY wakeup
STA    P_18H_WakeUpCtrl
```

Step 6: Latch PortA and stop CPU clock

```
LDA    P_08H_PortAData      ; latch PortA data
LDA    #07H                 ; stop CPU clock
STA    P_04H_CPUClkCtrl
NOP
NOP
NOP
```

13. Timer/Counter

GPLB3X provides two 16-bit re-loadable timers: TM0 and TM1. TM0 can be either timer or counter, but TM1 can only be a timer. A general diagram is illustrated as follows:



13.1. P_0CH_TimeBaseSelect (\$0C)(R/W)

P_TimeBaseSelect		0x0C		Interrupt time Base Selection				
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	TBL0	TBL1	TBH0	TBH1
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
3 : 2	TBL	W	Time base low clock selection	00= 2Hz 01= 8Hz
		R	Read Time base low clock status	10= 4Hz 11= 16Hz
1 : 0	TBH	W	Time base high clock selection	00= 128Hz 01= 512Hz
		R	Read Time base high clock status	10= 256Hz 11= 1KHz

To set timer:

- Step 1: Initial value of timer, first load low byte and the high byte. (\$10, \$11 or \$14, \$15)
- Step 2: Set timebase select port (\$0C)
- Step 3: Select clock source. (\$0F)
- Step 4: Enable timer interrupt. (\$01)

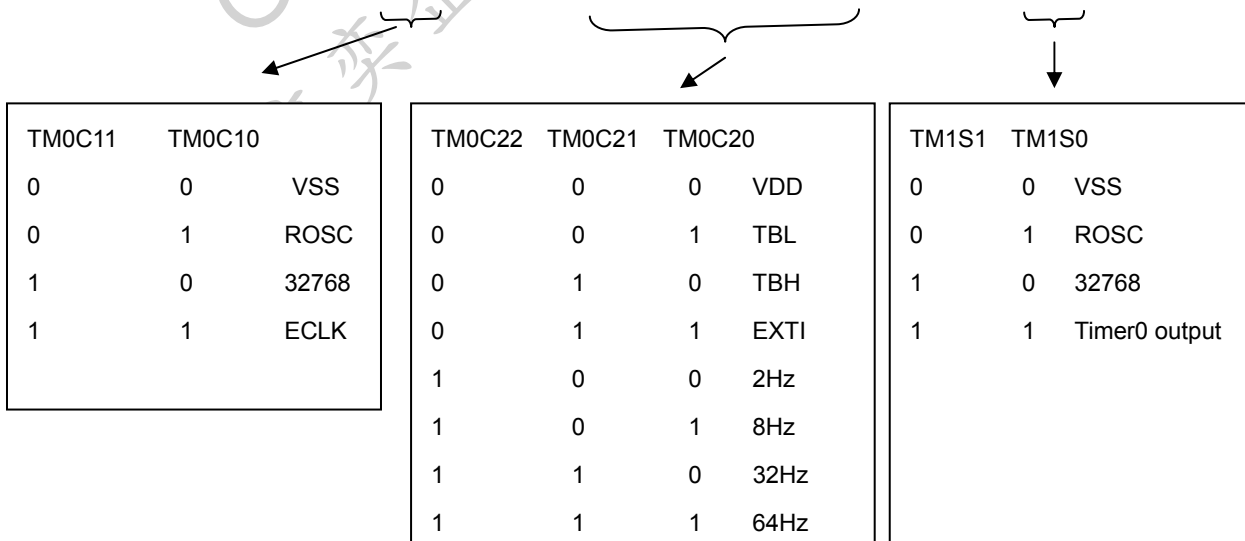
13.2. P_0FH_TimerCtrl (\$0F) (W)

P_TimerCtrl		0x0F			Timer Clock Selection			
Bit	7	6	5	4	3	2	1	0
Function	-	TM0C11	TM0C10	TM0C22	TM0C21	TM0C20	TM1S1	TM1S0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
6 : 2	TM0 Source	W	Timer0 clock source selection	See below table
		R	Read Timer0 clock source status	
1 : 0	TM1 Source	W	Timer1 clock source selection	See below table
		R	Read Timer1 clock source status	

Timer/Counter Control

	b7	b6	b5	b4	b3	b2	b1	b0
W	-	TM0C11	TM0C10	TM0C22	TM0C21	TM0C20	TM1S1	TM1S0



13.3. P_10H_TM0LowByte (\$10)(R/W)

P_TM0LowByte			0x10		Timer0 Low Byte Data			
Bit	7	6	5	4	3	2	1	0
Function	b7	b6	b5	b4	b3	b2	b1	b0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	TM0 low byte data	W	Write timer0 low byte	
		R	Read timer0 low byte	

Note: Unknown for default values; therefore, it must be initialized at beginning.

13.4. P_11H_TM0HighByte (\$11) (R/W)

P_TM0HighByte			0x11		Timer0 High Byte Data			
Bit	7	6	5	4	3	2	1	0
Function	b7	b6	b5	b4	b3	b2	b1	b0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	TM0 high byte data	W	Write timer0 high byte	
		R	Read timer0 high byte	

Note:

1. Unknown for default values; therefore, it must be initialized at beginning.
2. Since writing \$11 loads data into Timer0, data should be written into \$10 and then into \$11.

13.5. P_14H_TM1LowByte (\$14) (R/W)

P_TM1LowByte			0x14		Timer1 Low Byte Data			
Bit	7	6	5	4	3	2	1	0
Function	b7	b6	b5	b4	b3	b2	b1	b0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	TM1 low byte data	W	Write timer1 high byte	
		R	Read timer1 high byte	

Note: Unknown for default values; therefore, it must be initialized at beginning.

13.6. P_15H_TM1HighByte (\$15) (R/W)

P_TM1HighByte		0x15			Timer1 High Byte Data			
Bit	7	6	5	4	3	2	1	0
Function	b7	b6	b5	b4	b3	b2	b1	b0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	TM1 high byte data	W	Write timer1 high byte	
		R	Read timer1 high byte	

Timer1 High Byte Data Register and load Timer1 Data.

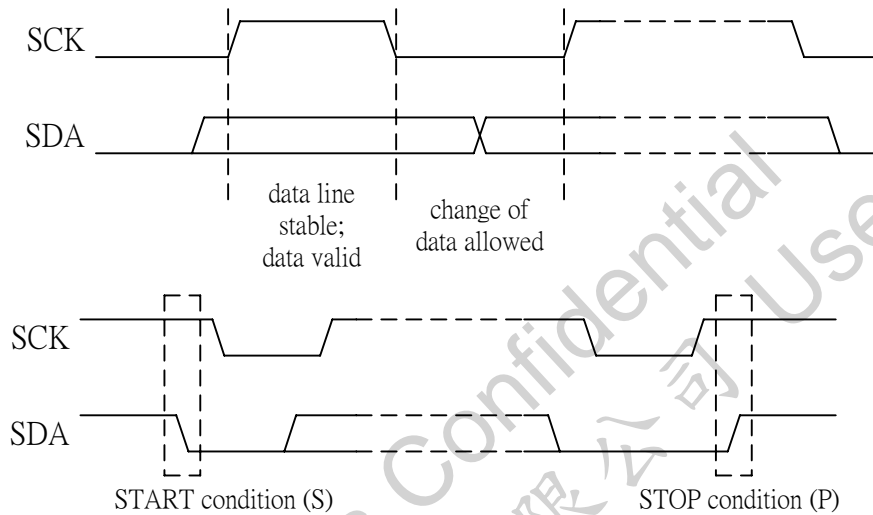
	b7	b6	b5	b4	b3	b2	b1	b0
R/W	b7	b6	b5	b4	b3	b2	b1	b0

Note:

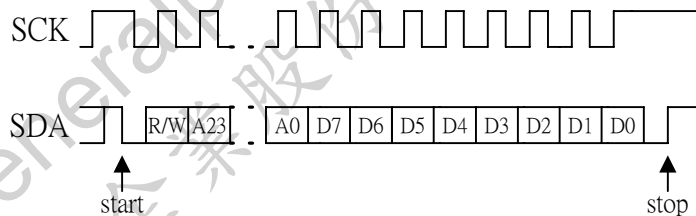
1. Unknown for default values; therefore, it must be initialized at beginning.
2. Since writing \$15 loads data into Timer1, data should be written into \$14 and then into \$15.

14. Serial SRAM Interface

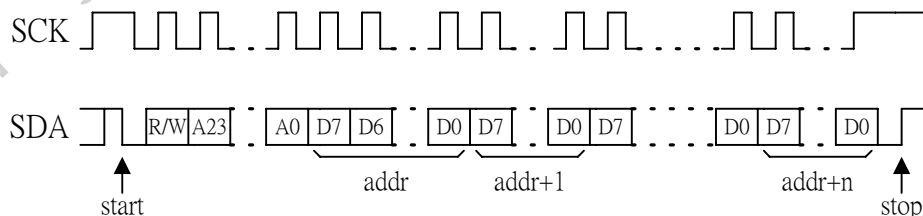
The Serial SRAM interface is able to expand the SRAM data storage. The Control Registers are ranged from \$30-\$36. Note that the pins of SDA and SCK are shared with PC [1:0] and therefore, users should define PC[1:0] as Serial SRAM interface by writing to Port \$27[1:0].



READ/WRITE Timing



Continuous READ/WRITE Timing



14.1. P_30H_Serial_SRAM_Data (\$30) (R/W)

P_Serial_SRAM_Data			0x30		Serial SRAM Data			
Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	Serial SRAM Data	W	Write Serial SRAM Data	
		R	Read Serial SRAM Data	

14.2. P_31H_Serial_SRAM_Addr1 (\$31) (R/W)

P_Serial_SRAM_Addr1			0x31		Serial SRAM Address1			
Bit	7	6	5	4	3	2	1	0
Function	M7	M6	M5	M4	M3	M2	M1	M0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	Serial SRAM Address1	W	Write Serial SRAM Address1	\$34[1:0]=10
		R	Read Serial SRAM Address1	

14.3. P_32H_Serial_SRAM_Addr2 (\$32) (R/W)

P_Serial_SRAM_Addr2			0x32		Serial SRAM Address2			
Bit	7	6	5	4	3	2	1	0
Function	M15	M14	M13	M12	M11	M10	M9	M8
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	Serial SRAM Address2	W	Write Serial SRAM Address2	\$34[1:0]=00 or \$34[1:0]=11
		R	Read Serial SRAM Address2	

14.4. P_33H_Serial_SRAM_Addr3 (\$33) (R/W)

P_Serial_SRAM_Addr3			0x33		Serial SRAM Address3			
Bit	7	6	5	4	3	2	1	0
Function	M23	M22	M21	M20	M19	M18	M17	M16
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	Serial SRAM Address3	W	Write Serial SRAM Address3	\$34[1:0]=11
		R	Read Serial SRAM Address3	

14.5. P_34H_S_SRAM_Control(\$34)(R/W)

P_Serial_SRAM_Control		0x34			Serial SRAM Clock/Address Control			
Bit	7	6	5	4	3	2	1	0
Function	Enable	R/W frame	Send R/W bit	CLKSEL1	CLKSEL0	-	AD_SEL1	AD_SEL0
Default	0	0	0	0	0	X	0	0

X: Unknow

Bit	Function	Type	Description	Condition
7	Serial Interface	W	Enable/Disable Serial Interface	0= disable
		R	Read Serial Interface status	1= enable
6	R/W frame	W	Start Frame for read/write	0= read
		R	Read Start Frame status	1= write
5	Send R/W bit	W	Read/Write bit frame applied	0= has R/W bit frame
		R	Read R/W bit frame status	1= no R/W bit frame
4 : 3	CLKSEL	W	System clock selection	00= System Clock/8 01= System Clock/2
		R	Read System clock status	10= System Clock/4 11= System Clock/16
1 : 0	AddrSEL	W	Address selection	00= Address=16(A15~A0) 01= No address
		R	Read Address status	10= Address=8(A7~A0) 11= Address=24(A23~A0)

14.6. P_35H_Serial_SRAM_Start (\$35) (R/W)

P_Serial_SRAM_Start		0x35			Serial SRAM Start Port to Enable Data Transfer			
Bit	7	6	5	4	3	2	1	0
Function	BUSY	-	-	-	-	-	-	-
Default	0	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:0	enable data transfer	W	Write start port to enable data transfer	Read 1= working Read 0= transfer completed
7	BUSY	R	Read Serial SRAM working status	

14.7. P_36H_Serial_SRAM_Stop (\$36) (W)

P_Serial_SRAM_Stop			0x36		Serial SRAM Stop Data Transfer			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	-	-	-	-
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:0	disable data transfer	W	Write data to Stop data transfer	

14.8. Serial Interface Program Example

```

;=====
;Serial interface
;=====

// 1.If serial SRAM interface is used, the following instructions are required after RESET
    % Set_CS_Pin_Low                ; when system reset, set CS pin to low
    STA    P_36H_SerialSRAM_StopPort ; when system reset, stop serial SRAM
    LDA    #%0000001x                ; set PortC bit0,1 as serial SRAM SCK,SDA
    STA    P_27H_CDConfig
    ....

// 2. Write to serial SRAM sequentially:
    LDA    #03H                      ; low address = 03
    STA    P_31H_SerialSRAM_Addr1
    LDA    #05H                      ; high address = 05
    STA    P_32H_SerialSRAM_Addr2
    LDA    #%11010000                ; Write mode, clk=CPUclk/4, 16 bit address
    STA    P_34H_SerialSRAM_Control
    STA    P_35H_SerialSRAM_StartPort ; start serial SRAM data transfer
    LDA    #55H                      ; write 55H to $503
    STA    P_30H_SerialSRAM_Data
    JSR    F_Chk_Transfer_Complete   ; wait transferring completely
    LDA    #AAH                      ; write AAH to $504
    STA    P_30H_SerialSRAM_Data
    JSR    F_Chk_Transfer_Complete   ; wait transferring completely
    STA    P_36H_SerialSRAM_StopPort ; stop data transfer

3.Read from serial SRAM sequentially:
    LDA    #03H                      ;low address = 03
    STA    P_31H_SerialSRAM_Addr1
    LDA    #05H                      ;high address = 05
    STA    P_32H_SerialSRAM_Addr2
    LDA    #%10010000                ;Read mode, clk=CPUclk/4, 16 bit address
    STA    P_34H_SerialSRAM_Control
    STA    P_35H_SerialSRAM_StartPort ;start serial SRAM data transfer
    LDA    P_30H_SerialSRAM_Data     ;clear serial SRAM data in buffer
    JSR    F_Chk_Transfer_Complete   ; wait transferring completely
    LDA    P_30H_SerialSRAM_Data     ;Read $503 Data(must be 55H)
    JSR    F_Chk_Transfer_Complete   ; wait transferring completely

```

```
LDA    P_30H_SerialSRAM_Data    ;Read $504 Data(must be AAH)
JSR    F_Chk_Transfer_Complete  ; wait transferring completely
STA    P_36H_SerialSRAM_StopPort ;stop data transfer
```

F_Chk_Transfer_Complete:

L_ChkLoop:

```
LDA    P_35H_SerialSRAM_StartPort ;check bit 7 busy flag
BMI    L_ChkLoop
RTS
```

Note1: After data transfer is finished, write to \$36 to stop Serial SRAM to save power consumption.

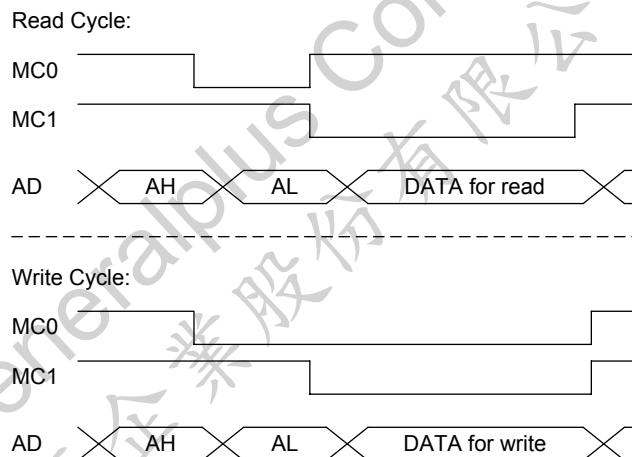
Note2: If \overline{CS} Pin of GPRSXXX connect to GND always, user must add a dummy Read or Write when system reset to initialize GPRSXXX.

15. Bus Memory Interface

A built-in bus memory interface is available on GPLB30/31/34/35/36/39. Through the use of bus memory interface, users can expand the memory capacity by using an external bus memory (SRAM, mask ROM or Flash). The bus memory interface includes 10 signal pins: MC1, MC0, and AD BUS [7:0] (shared with PortC.0, PortC.1, and Port B). Before using the bus memory interface, users should set MEXT=1 (\$03.7) and BANK register (\$00), then access address \$4000-BFFF to read or write data from external bus memory. Note that when using bus memory interface, CPU clock setting can not be set as $F_{OSC}/1$, it should be $/2$ or slower.

MC1	MC0	AD BUS [7:0]
L	L	Data for Write
L	H	Data for Read
H	L	AL (Address Low byte)
H	H	AH (Address High byte)

The simple timing relation is as follows:



Important Note: When BUS extender interface is enabled, PC.0 and PC.1 should be configured as MC0 and MC1. PortB should be set as AD BUS. In other words, PB 0~7, PC0, PC1 cannot be used for other purposes. Certainly, if BUS extender is used, users need another emulation board with GPBA to co-work with GPLB3X.

\$00.7: Bank Selection Register

Switching bank External (1) / Internal (0) Memory switch bit (on window \$4000~\$BFFF)

\$03.7: MEXT

Bus Memory Interface Enable Bit Control

\$0B.1: EXC

Common bank External (1) / Internal (0) Memory switch bit (on window \$C000~\$FFFF is interrupt vector).

EXC = 1, \$C000~\$FFFF at External Memory

EXT = 0, \$C000~\$FFFF at Internal memory

15.1. P_03H_BexMext (\$03)(W)

P_BexMext		0x03			Bus Interface Enable Control			
Bit	7	6	5	4	3	2	1	0
Function	MEXT	-	-	-	-			
Default	0	X	X	X	X	X	X	X

X: unknown

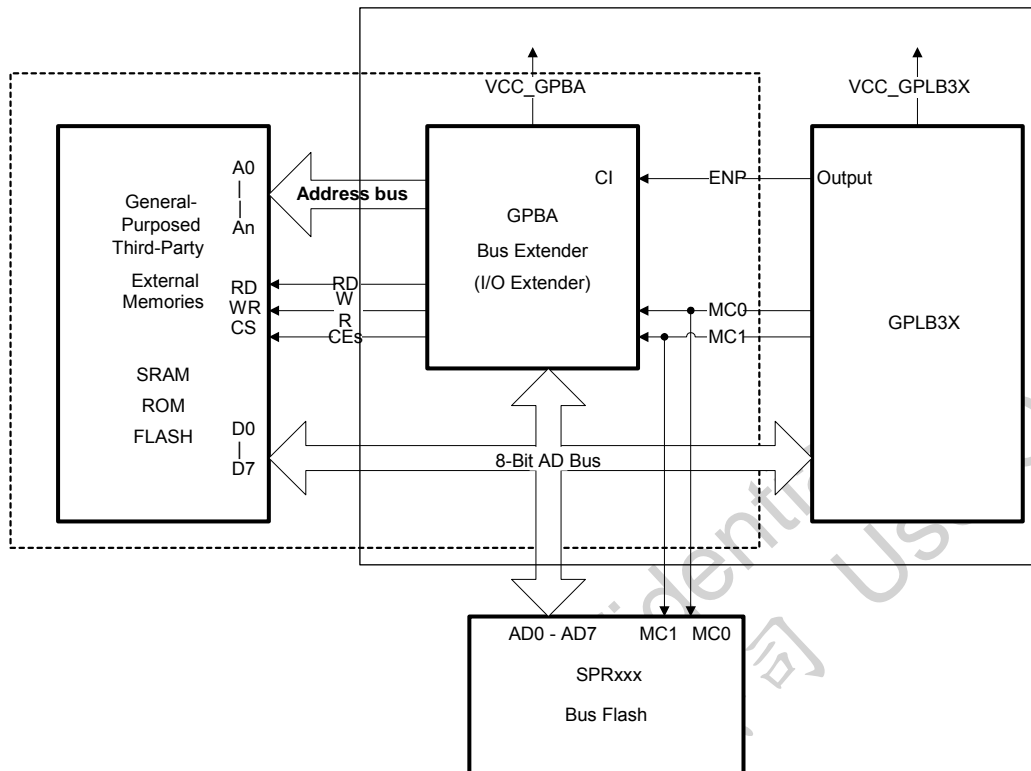
Bit	Function	Type	Description	Condition
7	MEXT	W	Bus Memory Interface Enable Bit Control	1 : Enable 0 : Disable

15.2. P_0DH_BMIVolumeID (\$0D)(W)

P_BMIVolumeID		0x0D			Bus Memory Volume ID Setup & Selection			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	-	VID2	VID1	VID0
Default	X	X	X	X	X	X	X	X

X: unknown

Bit	Function	Type	Description	Condition
2 : 0	VID	W	Define Bus memory Volume ID, give every memory a number	



GPLB3X bus memory interface.

- The area in solid line can be viewed as a micro-controller with address bus.
- The area in dash line can be viewed as the memory within the bus extender.

15.3. GPBA01 Bus Extender

Bus extender (BEX) plays a role as an interface between GPLB3X and general-purposed (third-party) memory products. In fact, the BEX is a decoder that decodes the signal on the AD bus of BMI to the general-purposed memory products. On the other hand, GPBA01 can be used as an I/O-extender.

There are 11 pins connected from GPLB3X to BEX except MC0, MC1, and AD bus. In addition, there is another pin named CI, the Cascade-In of BEX. When CI goes from low to high, the BEX will be reset and must be setup. When accessing BEX, the CI pin must keep at logical high level. Because there is no dedicated pin for BEX on GPLB3X, users can apply I/O pins to control it or connect CI pin to V_{CC} directly.

Both CI and CO provide the circuitry to concatenate up to seven BEX. In such case, the CO (Cascade-Out) of the former BEX is connected to the CI of next BEX to form a daisy-chain. After CI goes from low to high, the 1st setting of Volume ID (setting Register\$0D) will apply to the 1st BEX. After the 1st BEX is configured, it will rise its CO. The CO of the 1st BEX is connected with the CI of the 2nd BEX; as a result, the configuration will apply to the 2nd BEX, and...etc.

After setting Volume ID, any writing activity to Register\$0D will be taken as "selecting". For example, after setting the Volume ID of the BEX as 1,2,3,...(up to 7), simply write 3 to Register\$0D to select and access it when GPLB3X intends to access BEX of ID 3.

Note that the sequence of ID is not necessary of 1, 2, 3...7. The user is allowed to set the IDs as 3,2,1... or 7, 2, 4... Just keep in mind that the 1st ID is applied to the 1st BEX in the daisy chain.

15.4. P_20H_BEXPort0 (\$20)(R/W)

P_BEXPort0		0x20			Extender Port0			
Bit	7	6	5	4	3	2	1	0
Function	XP0.7	XP0.6	XP0.5	XP0.4	XP0.3	XP0.2	XP0.1	XP0.0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	XP0	W	I/O Extender Port0	

15.5. P_21H_BEXPort1 (\$21)(R/W)

P_BEXPort1		0x21			Extender Port1 & Function Control			
Bit	7	6	5	4	3	2	1	0
Function	XP1.7 OSCE	XP1.6 ICKOE	XP1.5 IPS1	XP1.4 IPS0	XP1.3 FAST	XP1.2 RSL2	XP1.1 RSL1	XP1.0 RSL0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	XP1	R/W	I/O Extender Port1	
7	OSCE	W	Infrared oscillator enable	
6	ICKOE	W	Infrared clock output enable	
5 : 4	IPS	W	Infrared pre-scalar counter	
3	FAST	W	Memory access time	0= Memory access with short chip select time for normal memory 1= Memory access with long chip select time for slow memory (default)
2 : 0	RSL	W	RAM volume selector	

15.6. P_22H_BEXPort2 (\$22)(R/W)

P_BEXPort2		0x22			Extender Port2 & IR Counter Preload \$ IR Counter			
Bit	7	6	5	4	3	2	1	0
Function	XP2.7 IRC7	XP2.6 IRC6	XP2.5 IRC5	XP2.4 IRC4	XP2.3 IRC3	XP2.2 IRC2	XP2.1 IRC1	XP2.0 IRC0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	XP2	R/W	I/O Extender Port2	
	IRC	W	IR Counter Preload	

15.7. P_23H_BEXConfig (\$23)(W)

P_BEXConfig		0x23			Bus Extender Configuration			
Bit	7	6	5	4	3	2	1	0
Function	CFG2	CFG1	CFG0 XP55	DIR2	DIR1	DIR03	DIR01	DIR00
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 5	CFG XP55	W	Bus extender configuration Extender Port55 output bit	

Bit	Function	Type	Description	Condition
4	DIR2	W	Extend Port2 control	0= input 1= output
3	DIR1	W	Extend Port1 control	0= input 1= output
2	DIR03	W	Extend Port0[7:3] control	0= input 1= output
1	DIR01	W	Extend Port0[2:1] control	0= input 1= output
0	DIR00	W	Extend Port0.0 control	0= input 1= output

Note:

1. When \$0A, \$0B.1 and \$0B.0 are used by bus extender, these bits must be kept floating. Do not modify the contents in these bits. Also, declare the \$0A as input mode with pull low state.
2. XP55 is available for output only if CFG[2..1]=0.
3. If the extend port is configured as input, there will be an internal pull-low resistor (37K Ohms @ VDD=5V or 78K Ohms @ VDD=3V).

15.7.1. Bus Extender Pin Assignment for 8 Configurations

Pins Name	Configuration Register \$23[7:5]							
	000	001	010	011	100	101	110	111
XP00	XP00	XP00	XP00	B0	B0	B0	B0	B0
XP01	XP01	XP01	XP01	B1	B1	B1	B1	B1
XP02	XP02	XP02	XP02	B2	B2	B2	B2	B2
XP03	XP03	XP03	XP03	B3	B3	B3	B3	B3
XP04	XP04	XP04	XP04	B4	B4	B4	B4	B4
XP05	XP05	XP05	XP05	B5	XP05	B5	XP05	B5
XP06	XP06	XP06	XP06	B6	XP06	B6	$\overline{CE2}$	$\overline{CE2}$
XP07	XP07	XP07	XP07	XP07	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$
XP10	XP10	XP10	A0	A0	A0	A0	A0	A0
XP11	XP11	XP11	A1	A1	A1	A1	A1	A1
XP12	XP12	XP12	A2	A2	A2	A2	A2	A2
XP13	XP13	XP13	A3	A3	A3	A3	A3	A3
XP14	XP14	XP14	A4	A4	A4	A4	A4	A4
XP15	XP15	XP15	A5	A5	A5	A5	A5	A5
XP16	XP16	XP16	A6	A6	A6	A6	A6	A6
XP17	XP17	XP17	A7	A7	A7	A7	A7	A7
XP20	XP20	XP20	A8	A8	A8	A8	A8	A8
XP21	XP21	XP21	A9	A9	A9	A9	A9	A9
XP22	XP22	XP22	A10	A10	A10	A10	A10	A10
XP23	XP23	XP23	A11	A11	A11	A11	A11	A11
XP24	XP24	XP24	A12	A12	A12	A12	A12	A12
XP25	XP25	XP25	A13	A13	A13	A13	A13	A13
XP26	XP26	XP26	A14	A14	A14	A14	A14	A14
XP27	XP27	XP27	$\overline{CE0}$	$\overline{CE0}$	$\overline{CE0}$	$\overline{CE0}$	$\overline{CE0}$	$\overline{CE0}$
Total I/O	25	25	8	1	2	0	1	0

Pins Name	Configuration Register \$23[7:5]							
	000	001	010	011	100	101	110	111
Available								
No. of Memories available	0	0	1	1	2	2	3	3

15.7.2. Memory Mapping Summary with Configuration 2~7

Mapping Address	Bank Select Value (\$00)	Mode	Chip Selection
\$8000~\$BFFF \$4000~\$7FFF (total: 32K)	1XXXXXXX	CFG=2	Access 32K Memory with /CE0
	1BBBBBBB	CFG=3	Access 4M Memory with /CE0
	10BBBBBB	CFG=4	Access 1M Memory with /CE1
	11BBBBBB	CFG=4	Access 1M Memory with /CE0
	1BBBBBBB	CFG=5	Access 4M Memory with /CE1
	100BBBBB	CFG=6	Access 1M Memory with /CE2
	101BBBBB	CFG=6	Access 1M Memory with /CE1
	11XBBBBB	CFG=6	Access 1M Memory with /CE0
	10BBBBBB	CFG=7	Access 2M Memory with /CE2
	11BBBBBB	CFG=7	Access 2M Memory with /CE1
\$C000~\$FFFF (total: 16K)	XXXXXXXX	CFG=2	Access second 16K Memory with /CE0
		CFG=3	
		CFG=4	Access second 16K Memory with /CE1
		CFG=5	
		CFG=6	Access second 16K Memory with /CE2
		CFG=7	

Note1: "B" is for extender memory bank select; "KB" means K-byte and "MB" for M-byte.
Note2: \$C000~\$FFFF is available while MEXT=1 and EXC (\$0B.1)=1. If program code is in \$C000~\$FFFF, EXC (\$0B.1) should always be "0". When \$C000~\$FFFF is mapped (the common ROM area is replaced), the program can be externally executed.
Note3: "X" means "don't care" which has no effect on bank selection.

15.8. Bus Extender Configuration

Step 1: Set MEXT bit (\$03.7)

Step 2: Set CI Pin to high

(GPBA CI pin is named "BEXEN" on GPLB3X emulation board. Users can apply an output pin to control BEXEN pin to enable/disable GPBA or connect V_{CC} to BEXEN to enable GPBA directly.)

Step 3: Setup "Nonzero" Volume ID (Write \$0D)

(After CI goes High, Volume-ID Port can be written, but it can be SETUP once only. Any other writing

command to Volume-ID Port will be considered as Volume SELECT)

(After Nonzero Volume ID is set, CO pin goes High for concatenation configuration)

Step 4: Setup Configuration (0~7) of the Volume (Write \$23[7..5])

Step 5: Enable EXC for corresponding Memory mapping access if necessary (refer to **Memory Mapping**).

Note: If external RAM is used, RAM Volume (RSL [2..0]) must be EQUAL to the BEX volume ID. For more detail of Bus Extender configuration and control, refer to GPBA01B Data Sheet.

15.9. Program Example

```

%PullBEXENLow                ; control pin CI to low
LDA    #%00xxxx01
STA    P_27H_PortCD_Control    ; Set PC[1:0] as bus interface control bit MC1,MC0
LDA    #80H                    ; Step 1: MEXT = 1
STA    P_03H_BexMext

%PullBEXENHigh                ; control pin CI to high (enable)
LDA    #1                       ; Step 3: Setup BEX Volume ID = 1
STA    P_0DH_BexVolID

LDA    #%110XXXXX              ; Step 4: Set as configuration=6 , $23[7:5]
STA    P_23H_BEXConfig

LDA    #%XXXXX001              ; Step4.1: Set RAM Volume the same as
STA    P_21H_BEXPort1          ; BEX Volume ID.

.....
(Setup second, third ...cascaded BEX if necessarily)
.....

LDA    #1                       ;Select memory of Volume ID = 1
STA    P_0DH_BMIVolumeID

```

Note: Before configuring BUS extender interface, set PortB as pull-low input, and PortC.0 and PortC.1 as BUS extender MC1, and MC0. In addition, %PullBEXENLow and %PullBEXENHigh are macros that control the high or low for output pin, which is interconnected to BEXEN (GPBA's CI).

15.10. IR Clock Setting

OSCE	ICKOE	OSCO	ICLK
0	X	H	L
1	0	Freq1	L
1	1	Freq1	Freq2

Note1: Freq1 is dependent on crystal of bus extender
Note2: $Freq2 = freq1 / (m * n * 2)$, where $n = 2^{IPS[1:0]}$ ($\$21[4:5]$), $m = 256 - IRCounterPreload(\$22)$
Note3: OSCO can only be probed as CFG=0 and CFG=1

Program Example

step 1: Connect crystal to XTAL1(pin #59) and XTAL2(pin #60) on bus extender, suppose 1.8MHz

step 2: Initialize GPLB3X

step 3: Setup BEX

```
LDA    #01H
STA    P_27H_PortCD_Control
LDA    #80H                ;set MEXT=1
STA    P_03H_BexMext
LDA    #01H
STA    P_0DH_VolumeID     ;set volume ID=1
LDA    #%110xxxxx        ;Set as configuration6(CFG=6)
STA    P_23H_BEXConfig
LDA    #01H
STA    P_0DH_VolumeID     ;select BEX volume ID=1
```

step 4: Setting the frequency of IR clock

```
LDA    #E8H                ;Set IRCounterPreload=E8H=232, set IPS[0:1]=0
STA    P_22H_BEXPort2     ;m=256-232=24

LDA    #%1100xxxx        ;Enable OSCE and ICKOE, set IPS[0:1]=0
STA    P_21H_BEXPort1     ;n=2^(IPS[0:1])=2^0=1
                                ;ICLK=Freq2=Freq1/(2*m*n)=1.8MHz/(2*24*1)=37.5kHz
```

step 5: Start to translate IR stream

```
LDA    #80H                ;
STA    P_21H_BEXPort1     ;
%IrOutputLowTime         ;the time ICLK output low

LDA    #C0H                ;
STA    P_22H_BEXPort2     ;
%IrOutputHighTime        ;the time ICLK output with Freq2(37.5kHz)
.....
```

Note:

1. OSCO (external memory output –enable signal) and ICLK (CLKO) is Clock divider output .
2. When IR function is applied, the IR clock setting registers IPS [0:1] and IRCOUNTERPRELOAD are shared with \$21[4:5] and \$22[0:7]. It conflicts with BEX I/O port XP1 [4:5] and XP2 [0:7] as CFG=0 and CFG=1. As a result, IR function and I/O port XP1 [4:5] and XP2 [0:7] couldn't be used at the same time as CFG=0 and CFG=1.

15.11. GPR1024 Bus Flash

GPR1024 Bus Flash is a 1M-bit flash memory that contains a BMI as the interface to GPLB3X. The memory mapping configuration is determined by external configuration pins CF[4:0]. The available configurations are listed as follows.

BMI Type	CF2	CF1	CF0	Volume ID \$0D[1:0]
A	0	0	0	00
C	0	1	0	01
E	1	0	0	xx
G	1	1	0	01

GPR1024 CF[2:0] configuration of BMI mode.

Type	CF4	CF3	Bank Switch
A, C, E	0	0	00XXXX bb
	0	1	01XXXXbb
	1	0	10XXXXbb
	1	1	11XXXXbb
G	1	0	10XXXXbb
	1	1	11XXXXbb

GPR1024 CF[4:3] configuration of bank setting, "b" is for extender memory bank select.

Note:

1. GPR1024 provides a serial interface compatible with other GENERALPLUS serial memories. Please refer to GPR1024 datasheet for more information.
2. The sector size of GPR1024 is 1K byte.
3. The memory banks of GPR1024 is multiple mappings, e.g., bank 80, 84, 88, ... BC are mapping to the same bank; so are bank C0, C4, C8, ... FC.
4. There can be two GPR1024 connected to the GPLB3X at the same time. If one GPR1024 is configured as Type G mapping to bank 80~83, the other as Type G mapping to bank C0~C3, the two GPR1024 can function normally. If this is the case, they share the same volume ID.
5. When using GPR1024, the volume ID must exactly be set as the table. For example, if using Type A, the volume ID[0:1] of GPR1024 must be 0 (i.e. \$0D=xxxxxx00).

Program Example

```

;initialize GPLB3X and GPR1024
; for more detail ,please prefer to GPR1024 data sheet
; CF[4:0] of GPR1024 = 10110 ( bounding option)
; Read sequence

LDA    #01H
STA    P_27H_PortCD_Control
LDA    #80H                ;set MEXT=1
STA    P_03H_BexMext
LDA    #01H

```

```

STA    P_0DH_VolumeID    ;set volume ID=1 for tape G
LDA    #80H
STA    P_00H_Bank        ;set bank to flash bank

LDA    #F0H              ;write F0H to any valid address to return GPR1024 to normal
mode.
STA    4000H             ;(RESET)

L_WaitForReady:
LDA    4000H             ;read any valid address,
:
:

```

GPR1024 provides various operations such as byte-programming, page-programming, page-erasing, and mass-erasing, ...etc. Please refer to **GPR1024 datasheet** for more information.

15.12. Bus Extender (BEX) Co-exists with Bus Flash

The GPBA01 BEX can be used with GPR1024 bus flash (BF for short) at the same time. When using BEX and BF together, see the following notes.

1. The BEX and BF are connected to the same bus. That is, they share 10 pins, including MC0, MC1 and AD pins.
2. The BEX and BF must map to different memory banks. For example, BF maps to banks 80~83, and BEX to banks C0~CF, ...etc. As mentioned in previous sections, BF configuration is determined by its configuration pins while BEX is set by GPLB3X program.
3. BEX and BF must have different volume IDs. Because the BF only works with specific volume IDs, the BEX ID must be chosen and set carefully.
4. After CI goes from low to high, the first setting of ID will apply to BEX, not to BF. Therefore, you must set the ID other than the BF ID in the first ID setting.
5. The memory on BEX may need a different operating voltage with BF. It may have several voltage levels in a single system.

Program Example

```

; initialize bus extender first
LDA    #01H
STA    P_27H_PortCD_Control
LDA    #80H                ;set MEXT=1
STA    P_03H_BexMext
LDA    #02H                ;the first setting of $0D will apply to bus-extender
STA    P_0DH_VolumeID
LDA    #C0H
STA    P_23H_BEXConfig    ;set BEX as CFG=6
LDA    #02H
STA    P_21H_BEXPort1
; next initialize GPR1024
LDA    #01H                ;GPR1024 works only with ID=1
STA    P_0DH_VolumeID

```



```
LDA    #80H
STA    P_00H_BankSelect
LDA    #F0H                ;return to normal mode
STA    4000H
```

```
.....
; access BEX
```

```
LDA    #02H
STA    P_0DH_VolumeID
LDA    #C0H
STA    P_00H_BankSelect
```

```
.....
; access BF
```

```
LDA    #01H
STA    P_0DH_VolumeID
LDA    #80H
STA    P_00H_BankSelect
.....
```

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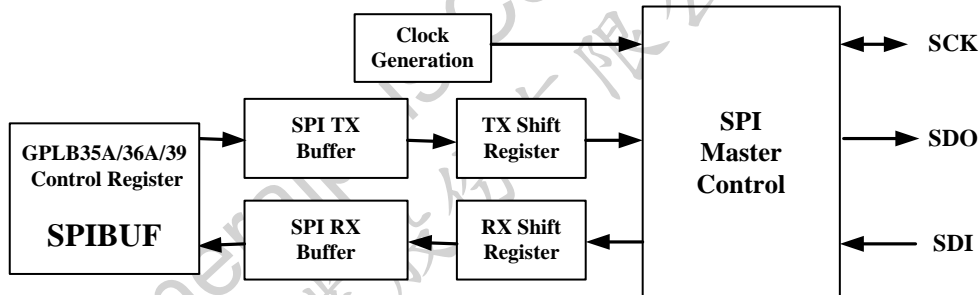
16. Serial Peripheral Interface (SPI)

16.1. Introduction

A Serial Peripheral Interface (SPI) controller is built in GPLB35/36/39 to facilitate communicating with other devices and components. There are three control pins on SPI, SPICK, SDI and SDO, which are shared with PortA.7, PortA.6 and PortA.5. These three pins cannot be GPIOs while SPI interface is enabled. In other words, any setting on corresponding GPIO control register will have no effect. The GPLB35/36/39 SPI features are listed as follows:

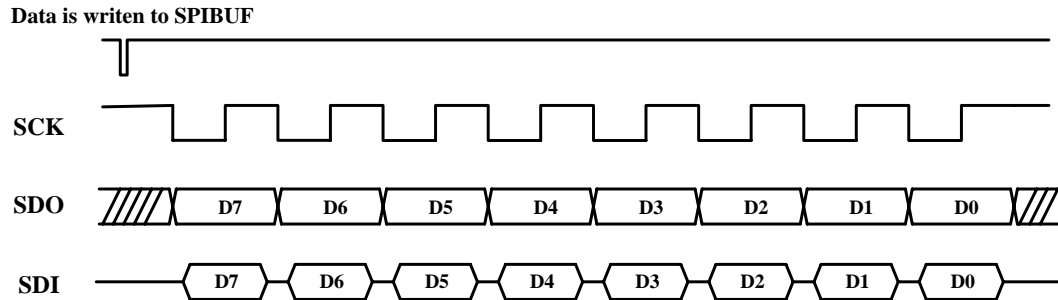
- Support only master mode.
- Support 4 byte (32 bits) SPI transmitting / receiving buffer.
- Programmable SPI clock frequency: System Clock /2, /4, /8, /16, /32, /64.

16.2. Master Mode Structure



The GPLB35/36/39 only supports master mode for SPI transmission and the function diagram is shown as above. As in the master mode, the shifting clock (SPICK) is generated by GPLB35/36/39. When software writes one byte through SPIBUF control register, the data is latched into its internal transmission buffer. After the SPI start/stop control register is cleared, the data will be started to transmit at the next SCK phase. The SPI shifts the data from MSB to LSB through the SDO pin. The 8-bit data is shifted out after 8 SCK cycles. At the same time, the data is also shifted in through slave device SDI pin. When each 8-bit transfer is completed, the SPIReady flag bit will be set.

In contrast, while GPLB35/36/39 received one byte successfully, the received data will be latched into receiving buffer and the SPIReady flag bit will be set. The following diagram depicts the timing scheme on SPI master mode. Note that the GPLB35/36/39 only provides the mode which polarity=1 and phase=1. That is, the slave device must be used as the same setting.



SPI timing scheme in GPLB35A/36A, Phase = 1 and Polarity = 1

16.3. SPI Control Pin Configuration

Name	I/O	Description
SPICK	O	Serial Peripheral Interface, Clock Pin (Shared with GPIO PortA.7)
SDO	O	Serial Peripheral Interface, Data Out Pin (Shared with GPIO PortA.5)
SDI	I	Serial Peripheral Interface, Data In Pin (Shared with GPIO PortA.6)

16.4. P_3008H_SPICTL0 (\$3008) (R/W)

P_SPICTL0		0x3008		SPI Clock/Transfer Byte Control				
Bit	7	6	5	4	3	2	1	0
Function	EN	SS	Countset1	Countset0	-	Clksel2	Clksel1	Clksel0
Default	0	1	0	0	-	0	0	0

Bit	Function	Type	Description	Condition
7	EN	W	Enable/Disable SPI Interface	0= disable
		R	Read SPI Interface status	1= enable
6	SS	W	Start/Stop Transmitted /received data	0= start
		R	Read Transmitted / received data status	1= stop
5 : 4	Countset	W	Transfer byte count	00= Transfer 1 byte per request 01= Transfer 2 byte per request
		R	Read Transfer byte status	10= Transfer 3 byte per request 11= Transfer 4 byte per request
2 : 0	Clksel	W	SPI Interface clock selection	000= System Clock/2 001= System Clock/4 010= System Clock/8

Bit	Function	Type	Description	Condition
		R	Read SPI Interface clock status	011= System Clock/16 110= System Clock/32 101= System Clock/64 11x= Reserved

Note:

1. If SPI interface is enabled (\$3008.7=1), PA5, PA6, PA7 will be SDO, SDI, SCK and cannot be used as GPIO.
2. The SPI start/stop transmitting control bit (\$3008.6) should be set to '0' at each transmission and will be reset to '1' after data transmission is completed.
3. Transfer 1 byte : P_3003H_SPI_TXD3 & P_3004H_SPI_RXD0 are used.
4. Transfer 2 byte : P_3003H_SPI_TXD3 , P_3002H_SPI_TXD2 & P_3005H_SPI_RXD1, P_3004H_SPI_RXD0 , are used. And then P_3003H_SPI_TXD3 is first byte of transfer byte. P_3005H_SPI_RXD1 is first byte of received byte.
5. Transfer 3 byte : P_3003H_SPI_TXD3 , P_3002H_SPI_TXD2 , P_3001H_SPI_TXD1& , P_3006H_SPI_RXD2, P_3005H_SPI_RXD1, P_3004H_SPI_RXD0 are used. And then P_3003H_SPI_TXD3 is first byte of transfer byte. P_3006H_SPI_RXD2is first byte of received byte.

16.5. P_3009H_SPICTL1 (\$3009) (R)

P_SPICTL1		0x3009			SPI Clock/Transfer Byte Control			
Bit	7	6	5	4	3	2	1	0
Function	-	-	-	-	-	-	-	SPIReady
Default	X	X	X	X	X	X	X	1

Bit	Function	Type	Description	Condition
0	SPIReady	R	Ready to transmit/receive data or not	0= not ready 1= ready

16.6. P_3000H_SPI_TXD0 (\$3000) (W)

P_SPI_TXD0~TXD3		0x3000~0x3003			SPI Transmitted Buffer			
Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	TXD	W	Transmitted buffer	\$3008[4:5]

16.7. P_3001H_SPI_TXD1 (\$3001) (W)

16.8. P_3002H_SPI_TXD2 (\$3002) (W)

16.9. P_3003H_SPI_TXD3 (\$3003) (W)

16.10. P_3004H_SPI_RXD0 (\$3004) (R)

P_SPI_RXD0~RXD3			0x3004~0x3007		SPI Received Buffer			
Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7 : 0	RXD	R	Received buffer	\$3008[4:5]

16.11. P_3005H_SPI_RXD1 (\$3005) (R)

16.12. P_3006H_SPI_RXD2 (\$3006) (R)

16.13. P_3007H_SPI_RXD3 (\$3007) (R)

16.14. Program Examples

```

// 1.Send the data to SPI buffer
F_SPI_Transmit:
    LDA    #00H
    STA    P_3000H_SPITXD0
    LDA    #FFH
    STA    P_3001H_SPITXD1
    LDA    #55H
    STA    P_3002H_SPITXD2
    LDA    #AAH
    STA    P_3003H_SPITXD3

// 2. Set SPI control register and start transmitting:
    LDA    #%101110000           ;SPICK = system clock/2, transfer 4 byte per request
    STA    P_3008H_SPICTL0

// 3.Check if the transmitting/receiving is completed:
L_Chk_SPI_Ready:
    LDA    P_3009H_SPICTL1       ;check SPIReady bit
    AND    #%00000001
    BEQ    L_Chk_SPI_Ready

// 4.The SPIReady and start/stop transmitting control bit ($3008.6) will be reset to '1' after data
transmission is completed.

```

17. Key Scan Port

GPLB3X supports key scan function. The LCD driver will generate a key strobe signal in the period of every common. When PA received this strobe signal, a wake-up is issued. Then, users can send the key scan signal through SEG[15:0] to determine the location of the depressed key.

17.1. P_3AH_Keyscan_Ctrl (\$3A) (R/W)

P_Keyscan_Ctrl		0x3A				Keyscan Control		
Bit	7	6	5	4	3	2	1	0
Function	R1ON	-	-	-	-	-	SCAN1	SCAN0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	R1ON	W	PortA pull-high/low degree	0= weak pull-high/low(240K/160K)
		R	Read PortA pull-high/low degree status	1= strong pull-high/low(60K/40K)
1	SCAN1	W	Enable/Disable SEG[15:8] key scan output	0= disable
		R	Read SEG[15:8] key scan output status	1= enable
0	SCAN0	W	Enable/Disable SEG[7:0] key scan output	0= disable
		R	Read SEG[7:0] key scan output status	1= enable

17.2. P_3BH_Keyscan_Port1 (\$3B)

P_Keyscan_Port1		0x3B				Output Key Scan Data		
Bit	7	6	5	4	3	2	1	0
Function	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	SEG[7:0]	W	SEG[7:0] functions as an output port data	\$3A.0=1

17.3. P_3CH_Keyscan_Port 2 (\$3C)

P_Keyscan_Port2		0x3C				Output Key Scan Data		
Bit	7	6	5	4	3	2	1	0
Function	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7 : 0	SEG[15:8]	W	SEG[15:8] functions as an output port data	\$3A.1=1

17.4. Key Scan Program Example

```

;=====
; KeyScan Program Example
; Ex: Using S0-S15 as keyboard scan output port and PortA as input pull-high.
; The recommended procedures are as follows:
;=====

Step0: Disable PortA strobe signal synchronized with LCD waveform
      LDA    #0
      STA    P_05H_PortAStrobePH
      TAX

Step1: Disable LCD strobe waveform
      LDA    #%XXXXXX0X
      STA    P_24H_LCD_Option_Setting

Step2: Send scan line to output port
      LDA    #SCAN_PATTERN1
      STA    P_3BH_Keyscan_Port1
      LDA    #SCAN_PATTERN2
      STA    P_3CH_Keyscan_Port2

Step3: Turn R1 on, enable keyboard scan output port S0 to S15
      LDA    #%1000011
      STA    P_3AH_Keyscan_Ctrl

Step4: Delay about 1us to ensure Segment[0:15] status is ready and read PortA
      %Dealy_1us
      LDA    P_08H_PortAData

Step5: Turn R1 off, disable keyboard scan output port S0 to S15
      STX    P_3AH_Keyscan_Ctrl

Step6: Enable PortA Strobe signal again
      LDA    #0FFH
      STA    P_05H_PortAStrobePH

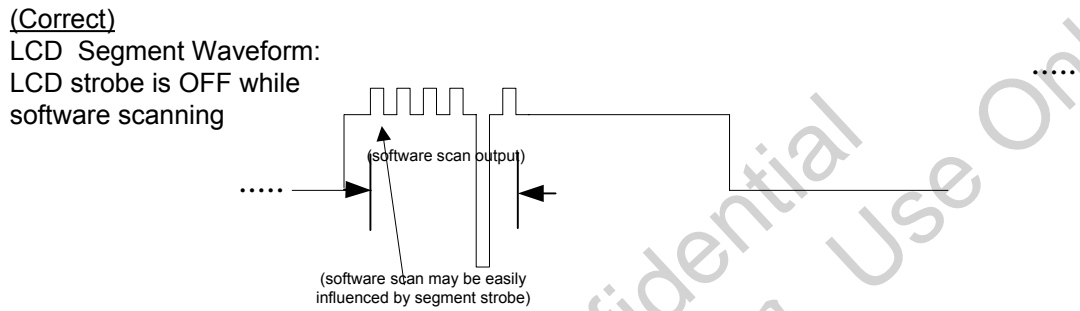
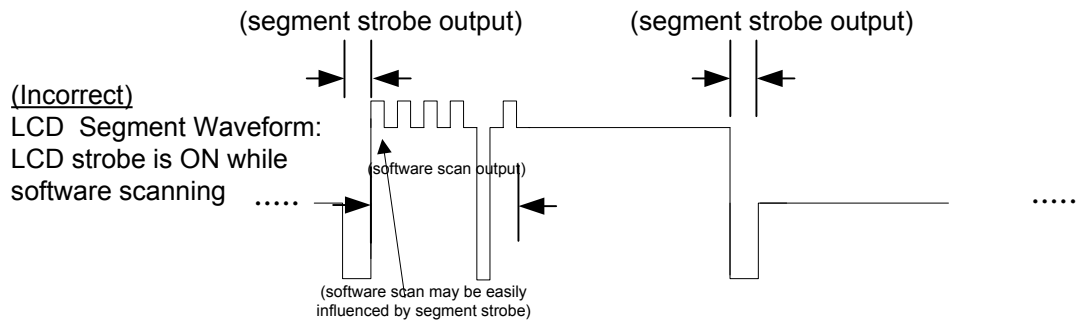
Step7: Key debounce

Step8: When leaving the key scan routine, make sure to enable LCD strobe waveform
      LDA    #%xxxxxx1x
      STA    P_24H_LCD_Option_Setting

```

Note:

1. When PortA is used for key-scan input port (pins), all pins for key-scan input must be configured as pull-high state.
2. The key scan routine should be as short as possible to prevent influencing LCD display.
3. In key scan routine, LCD strobe waveform (P_24H_LCD_Option_Setting.b1) must be disabled.



18. Bit Operation Port

GPLB3X provides two special bit operation ports for users to handle graphic pattern more conveniently.

18.1. P_3EH_Mirror_Byte (\$3E) (R/W)

P_Mirror_Byte		0x3E			Mirror Byte			
Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description								Condition
7 : 0	D[7:0]	W	D7	D6	D5	D4	D3	D2	D1	D0	
		R	D0	D1	D2	D3	D4	D5	D6	D7	

Example:

```
LDA #35H
STA P_3EH_Mirror_Byte
LDA P_3EH_Mirror_Byte ;acc=ACH
```

18.2. P_3FH_Swap_Nibble (\$3F) (R/W)

P_Swap_Nibble		0x3F			Data Swap			
Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description								Condition
7 : 0	D[7:0]	W	D7	D6	D5	D4	D3	D2	D1	D0	
		R	D3	D2	D1	D0	D7	D6	D5	D4	

Example:

```
LDA #35H
STA P_3FH_Swap_Nibble
LDA P_3FH_Swap_Nibble ;acc=53H
```

19. Voltage Detector/Low Voltage Reset

The voltage detector comprises a band-gap reference generator and a comparator. The band-gap reference generates a fixed voltage ($\approx 1.22V$) for comparator to sense a low voltage event. There are 8 programmable detection levels provided. Program can be written to monitor the Register \$39 for a low voltage event detection. In addition, users can also enable the LV NMI by programming Register \$38.

The detector checks VDD every 32Hz and takes 1/32768 second to sense the low voltage event. If the power supply voltage drops below the detection level, the NMI will be generated to inform CPU that the low voltage event occurs. To avoid multiple LV NMIs occur when unexpected noise interferes the power, only the first LV NMI will be generated and latched. No other LV NMIs will be accepted until LVDEN (\$39.7) is disabled (given "0") and enabled (given "1") afterward. The Low Voltage Reset (LVR) of GPLB3X is set to 2.20V. When VDD drops below 2.20V for more than 125ms (4 times of LVD samples), LVR will reset the device. The LVR of GPLB3X is a mask option.

Note: When 32KHz X'TAL and LVR mask options are both enabled, it is prohibited that CPU and 32KHz clock stop at the same time in sleep mode. That is, DON'T stop the 32KHz RTC clock when in sleep mode. Otherwise an unexpected reset may occur when CPU wakes up from sleep mode.

19.1. P_39H_LVD_Ctrl (\$39)(R/W) (Default: 0xxx0000)

P_LVD_Ctrl		0x39		Low Voltage Detector Control				
Bit	7	6	5	4	3	2	1	0
Function	LVDEN	-	LV Status	-	VDSEL	LVSEL2	LVSEL1	LVSEL0
Default	0	-	-	-	0	0	0	0

Bit	Function	Type	Description	Condition
7	LVDEN	W	Enable / Disable voltage detector	0= disable
		R	Read voltage detector status	1= enable
5	LV Status	R	Low voltage status	0= VDD<LV 1= VDD>LV
3	VDSEL	W	Low voltage detection range selection	0= 2.2V~2.9V
		R	Read Low voltage detection range status	1= 3.3V~3.45V
2 : 0	LVSEL	W	Low voltage detection level selection	See below table
		R	Read Low voltage detection level status	

LV Detection Level

LVSEL.2	LVSEL.1	LVSEL.0	VDSEL = 0	VDSEL = 1
0	0	0	N/A	3.30 V
0	0	1	N/A	3.45 V

LVSEL.2	LVSEL.1	LVSEL.0	<i>VDSEL = 0</i>	<i>VDSEL = 1</i>
0	1	0	2.40 V	3.60 V
0	1	1	2.50 V	3.75 V
1	0	0	2.60 V	3.90 V
1	0	1	2.70 V	4.05 V
1	1	0	2.80 V	4.20 V
1	1	1	2.90 V	4.35 V

Note:

1. The tolerance of LVD voltage is +/- 0.1V.
2. GPLB34/35/36 only support 2.4v-2.9v LVD level.

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20. LB39 EV Chip Ctrl

20.1. P_3034H_LB39B_EV_Chip_Ctrl (\$3034)(R/W) (Default: 00xx0000)

P_LB39B_EV_Chip_Ctrl		0x3034			LB39B EV Chip Control			
Bit	7	6	5	4	3	2	1	0
Function	X32KSEL	LVR OPT	-	-	-	REGENBOPT	REGOPT1	REGOPT0
Default	0	0	X	X	0	0	0	0

Bit	Function	Type	Description	Condition
7	X32KSEL	W	32768 crystal or 32K R _{OSC} selection	0= 32768 crystal
		R	Read clock source status	1= 32K R _{OSC}
6	LVR OPT	W	LVR option setting	0= disable
		R	LVR enable/disable status	1= enable
2	REGENBOPT	W	Voltage regular for external memory device	0= enable
		R	Read Voltage regular output for external memory device status	1= disable
1 : 0	REGOPT	W	Regulator output voltage selection	00= 2.7V 01= 3.0V
		R	Read Regulator output voltage status	10= 2.5V 11= 2.6V

*This register is only for GPLB39B emulation chip. (GPLB39B real chip is not suitable, also)

21. Watchdog Timer

21.1. Watchdog

An on chip WDT (Watchdog Timer) is available. The WDT is designed for recovering system from abnormal operation. During normal operation, a WDT generates a device RESET. The basic idea is that the WDT generates a reset signal every certain period of time (1 second for GPLB3X). The program should be designed to clear the WDT before the reset signal occurs. If a system is halt or not working properly for some reasons causing the WDT is not cleared within the time period, WDT will generate a reset signal to restart system. In GPLB3X, GENERALPLUS recommends to clear WDT every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing "55H" to address \$3031H. Note that the WDT only works when 32768 Hz clock is available.

P_Watch_Dog_Clear			0x3031		Watch Dog Timer Clear Port			
Bit	7	6	5	4	3	2	1	0
Function	WDOG							
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:0	WDOG	W	Write #55H to this port for clearing WDOG Timer	

21.2. Important Note to Watchdog Option on EMU Board

The watchdog option on EMU board cannot be enabled (EN) while downloading program into EMU board. Switching watchdog option to "EN" (enabled) while downloading program will cause CPU resets repeatedly. Thus, program cannot be downloaded into EMU board successfully. As a result, the watchdog on EMU board must be "DIS" (disabled) before (while) downloading program into EMU board. After download is completed, the watchdog option can be selected to "EN" (enabled) to perform the watchdog function.

22. Reset Flag

GPLB3X provides reset flag register to detect reset source .

If reset has been happened, corresponding bit of \$3030 will be set to '1' forever. Three methods for clear reset flag : power on reset or following two ways.

- i. Clear Reset Flag : It must write '30h' to \$303F first, then write '00h' to \$3030.

Ex:

```
LDA #30h
STA $303F
LDA #00h
STA $3030
```

- ii. Software Reset : It must write 'FFh' to \$303F first, then write 'FFh' to \$3030.

Ex:

```
LDA #FFh
STA $303F
LDA #FFh
STA $3030
```

P_Reset_Flag		0x3030						
Bit	7	6	5	4	3	2	1	0
Function	LVRST	WDRST	-	IL_AD	SWRST	-	-	-
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	LVRST	R	LVR reset	
6	WDRST	R	watchdog timer reset	
4	IL_AD	R	illegal address reset	
3	SWRST	R	software reset	
7:0	Flag clear	W	Write #00H to \$3030 for clearing all reset flag	After writing #30H to \$303F
7:0	Flag clear	W	Write #FFH to \$3030 for executing software reset	After writing #FFH to \$303F

23. Voltage Regulator

The GPLB30/31/34/35/36/39 provides the voltage regulator function and four voltage levels: 2.5V, 2.6V, 2.7V and 3.0V could be selected. It is used to supply a stable voltage for external devices which working voltage range is 2.5V-3.0V. **The voltage regulator does not pump system power VDD so that it will vary with VDD if VDD is lower than the regulator setting voltage.** When the function is applied, the following two selections must be set in the confirmation sheet.

1. VOLTAGE REGULATOR

- Enable
- Disable

2. REGULATOR OUTPUT SELECTION

- 2.5V
- 2.6V
- 2.7V
- 3.0V

Note:

1. The VROUT pin must be connected to VDD when internal regulator is disabled and connected with a capacitor 10uF when regulator is enabled.
2. If voltage regulator is optioned, the logical high level at PortB and PortC[1:0] are varied according to voltage regulator.

24. Compiling Procedures & ICE Usage

A. Compiling Procedure

It requires assembler, linker, HEXtoTSK(hex2tsk.exe) and GENERALPLUS binder(binbind.exe) for compiling program. The object of hex2tsk.exe is to transfer INTEL HEX file to TSK file (binary file) that can be accessible by GENERALPLUS binder. The two primary goals of GENERALPLUS binder is to bind some specified resource files on linked file, and to change a CPU-view file to a ROM file that can be released to GENERALPLUS. For the difference between CPU view and ROM view, refer to **Memory Mapping**.

The format to be recognized by GENERALPLUS binder after link procedure is the format of 64KB-CPU-view group. For a 128KB-program, there will be four 64KB-CPU-Views (Bank selection: 0,1,2,3) in the file (totally 256KB). The first 64KB is the CPU view when bank selection is 0; the second 64KB is the CPU view when bank selection is made to 1. The third 64KB is the CPU view when bank selection is 2 and the fourth 64KB is the CPU view when bank selection is 3.

The following two examples depict the compiling procedures. In general, if all programs (not resource files) are inside the common area (CPU View \$C800~\$FFFF), the first example is applied. If program size exceeds the common area (14KB), program should be resident in bank1, bank2 and bank3. We should involve linker with script file (.lnk) in this situation; this is so-called "Enhanced Data File mode" in 2500AD Software INC. The second example will roughly describe how it works. For more information, refer to **GPDC/GPL13X Binder User Guide**. Simply, this linker mode will generate a HEX file with 4 sets of 64K-CPU-View, totally 256KB.

Example :

Compile Procedure Batch File (.BAT)

```
X6502      demo.asm -D
L6502      demo.lnk
BINBIND    demo.snf
```

GENERALPLUS Binder Script File (.SNF)

```
.REM      SUNPLUS 2001-10-17
.BODY     SPLB3X
.OUTPUT   demo.BIN           ;define binbind.exe output file name
.SYMBOL   demo.SYM           ;identifies input symbol file
.FILE     demo.s37           ;input file
.FILL     00h                ; define data for reversed blank area
.SCOPE    3                  ; indicates which bank of start location of resource file.
.FROM     L_ProgramEnd       ; indicates start-location of resource files. Binbind.exe will put
                                resource data
.EXTERN    T_BitmapAddressTable
          {
            .PTR24 (
              BMP\apple.bin
              BMP\crab.bin
              BMP\sun.bin
            )
          }
.EXTERN    T_SpeechAddressTable
          { .PTR24 ( SPEECH\water.adp) }
.END
```

Linker script file (.LNK)

Version: 2001-10-17

Options: map, motorola s37, microtek

Input: demo
Output: demo
Group: code_group = CODE+Common

Locate: Bank0H at 8000h
Locate: code_group at C800h
Locate: INTVector at FFFAh
Locate: Bank1 at 14000h linked to 4000h
Locate: Bank2 at 24000h linked to 4000h
Locate: Bank3 at 34000h linked to 4000h

*map :Create .MAP file,
*containing link error, section summary
*Motorola s37: Define Output Code File Format
*Microteck: Define Symbol Table Format
*Names the input file(s) to be linked
*Names output file
*combines sections into a group to be linked as
*a single entity
*1st is Output Address, 2nd is Logical Address
*1st is ROM Address, 2nd is CPU View Address

Assembly file (.ASM)

```

.SYMBOLS                ;;Sends symbol information to the linker
.LINKLIST                ;;Makes the linker produce relocated listing file

;*****
Bank0H:                  .SECTION                ;;Creates "Bank0H" as a user-defined section (Size=16K)
.include                 files1.asm            ;;Logical Address: bank0: 0x8000~0xBFFF
:
:
                        .ENDS
;*****
Common:                  .SECTION                ;;Creates "Common" as a user-defined section (Size=8K)
RESET:                   ;;Program start
:
:
.include                 filesA.asm            ;;Logical Address: bank0: 0xC800~0xFFFF
.include                 filesB.asm
.include                 filesC.asm
:
:
T_BitmapAddressTable:
    DB                   0,0,0
    DB                   0,0,0
    DB                   0,0,0
T_SpeechAddressTable:
    DB                   0,0,0
                        .ENDS
;*****
INTVector:               .SECTION                ;;Creates "INTVector" as a user-defined section(Size=6B)
                        DW                   NMI            ;;Logical Address: bank0: 0xFFFFA~0xFFFF
                        DW                   RESET
                        DW                   IRQ
                        .ENDS
;*****
Bank1:                   .SECTION                ;;Defines Bank1 as a user-defined-section( Size=32KB)
.include                 files1-1.asm          ;;Logical Address: bank1: 0x4000~0xBFFF
.include                 files1-2.asm
.include                 files1-3.asm
:
:
                        .ENDS
;*****
Bank2:                   .SECTION                ;;Defines Bank2 as a user-defined-section( Size=32KB)
.include                 files2-1.asm          ;;Logical Address: bank2: 0x4000~0xBFFF
.include                 files2-2.asm
:

```

```

:
Bank3:      .ENDS
           .SECTION      ;;Defines Bank3 as a user-defined-section( Size=32KB)
           files3-1.asm  ;;Logical Address: bank3: 0x4000~0xBFFF
           files3-2.asm
           files3-3.asm
           files3-4.asm
:
:
L_ProgramEnd      ;;Notifies GENERALPLUS Binder from where to put
                  resource files.
;*****
;
:
:
           .ENDS
.END

```

B. ICE Usage

In ICE emulation, emulation memory inside ICE cannot be used. Therefore, ICE memory should be set as external (that means SRAM on emulation board is used) and readable/writeable. In addition, ICE clock should also be set as external (that means CPU clock comes from ROSC on emulation board). Note that GPLB3X emulation board with GENERALPLUS ICE may not work when VDD is below 3.6V. However, the emulation board stand-alone (without GENERALPLUS ICE) is able to run with VDD=2.4V~5.5V. Since GPLB3X is a full instruction CPU, ICE should be set as F6502.

Memory map from mask-ROM view is quite different from GPLB3X CPU view. The following ICE command script file depicts how to download a binary ROM code (demo.bin) into the SRAM on emulation board.

```

>X
>CPU F6502
>CLK EXT
>MS 0000 FFFF EXT
>MS 0000 FFFF RW
>O 0 0
>L demo.bin 0 7FFF 8000
>O 0 1
>L demo.bin 8000 BFFF 8000
>L demo.bin C000 FFFF 4000
>O 0 2
>L demo.bin 10000 13FFF 8000
>L demo.bin 14000 17FFF 4000
>O 0 3
>L demo.bin 18000 1BFFF 8000
>L demo.bin 1C000 1FFFF 4000
>X

```

25. Mask Options

GPLB30	GPLB31	GPLB32	GPLB33A
<p>1. 32768 OSCILLATOR — X'TAL — R-oscillator</p> <p>2. WATCHDOG TIMER — Enable — Disable</p> <p>3. PA [5:7]/ SEG [69:67] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>4. PB [0:7]/ SEG [64:57] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>5. PC [2:3]/Tx, Rx/ SEG [66:65] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>6. PC [4:7]/ SEG [56:53] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>7. PD [0:4]/ SEG [52:48] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>8. Voltage regulator.</p> <p>9. LVR (Low Voltage Reset)</p>	<p>1. 32768 OSCILLATOR — X'TAL — R-oscillator</p> <p>2. WATCHDOG TIMER — Enable — Disable</p> <p>3. PA [3:7]/ SEG [73:69] — Each port/segment can be optioned as I/O or LCD segment output individually.</p> <p>4. PC [4:7]/ SEG [68:65] — Each port/segment can be optioned as I/O or LCD segment output individually.</p> <p>5. PD [0:4]/ COM [31:27] — Each port/common can be optioned as I/O or LCD common output individually.</p> <p>6. Voltage regulator.</p> <p>7. LVR (Low Voltage Reset)</p>	<p>1. 32768 OSCILLATOR — X'TAL — R-oscillator</p> <p>2. WATCHDOG TIMER — Enable — Disable</p> <p>3. AUDIO OUTPUT SELECT — PWM — DAC</p> <p>4. PA [6:7]/ SEG [63:62] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>5. PB [0:5]/ SEG [69:64]/ COM [21:16] — Each port/segment/common can be optioned as I/O or LCD segment/common individually.</p> <p>6. PC [0:1]/ SCK, SDA/ SEG [61:60] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>7. PC [4:7] / SEG [73:70] / COM [25:22] — Each port/segment/common can be optioned as I/O or LCD segment/common individually.</p> <p>8. PD [0:5]/ COM [31:26] — Each port/common can be optioned as I/O or LCD common individually.</p> <p>9. LVR (Low Voltage Reset)</p>	<p>1. 32768 OSCILLATOR — X'TAL — R-oscillator</p> <p>2. WATCHDOG TIMER — Enable — Disable</p> <p>3. PA [7]/ SEG [51] — Each port/segment can be optioned as I/O or LCD segment individually.</p> <p>4. PB [0:7]/ SEG [46:39] — Each port/segment can be optioned as I/O or LCD segment/common individually.</p> <p>5. PC [4:7] / SEG [50:47] — Each port/segment can be optioned as I/O or LCD segment/common individually.</p> <p>6. LVR (Low Voltage Reset)</p>

GPLB33B	GPLB34	GPLB35	GPLB36
1. 32768 OSCILLATOR — X'TAL — R-oscillator 2. WATCHDOG TIMER — Enable — Disable 3. PB [0:7]/ SEG [41:34] — Each port/segment can be optioned as I/O or LCD segment/common individually. 4. PC [2:7] / SEG [47:42] — Each port/segment can be optioned as I/O or LCD segment/common individually. 5. LVR (Low Voltage Reset)	1. 32768 OSCILLATOR — X'TAL — R-oscillator 2. WATCHDOG TIMER — Enable — Disable 3. Voltage regulator. 4. LVR (Low Voltage Reset)	1. 32768 OSCILLATOR — X'TAL — R-oscillator 2. WATCHDOG TIMER — Enable — Disable 3. Voltage regulator. 4. LVR (Low Voltage Reset)	1. 32768 OSCILLATOR — X'TAL — R-oscillator 2. WATCHDOG TIMER — Enable — Disable 3. Voltage regulator. 4. LVR (Low Voltage Reset)

GPLB37	GPLB39A/B
1. 32768 OSCILLATOR — X'TAL — R-oscillator	1. 32768 OSCILLATOR — X'TAL — R-oscillator
2. WATCHDOG TIMER — Enable — Disable	2. WATCHDOG TIMER — Enable — Disable
3. AUDIO OUTPUT SELECT — PWM — DAC	3. Voltage regulator. 4. LVR (Low Voltage Reset)
4. PA [6:7]/ SEG [63:62] — Each port/segment can be optioned as I/O or LCD segment individually.	
5. PB [0:5]/ SEG [69:64]/ COM [21:16] — Each port/segment/common can be optioned as I/O or LCD segment/common individually.	
6. PC [0:1]/ SCK, SDA/ SEG [61:60] — Each port/segment can be optioned as I/O or LCD segment individually.	
7. PC [4:7] / SEG [73:70] / COM [25:22] — Each port/segment/common can be optioned as I/O or LCD segment/common individually.	
8. PD [0:5]/ COM [31:26] — Each port/common can be optioned as I/O or LCD common individually.	
9. LVR (Low Voltage Reset)	

26. Control Register Summary

Address	Function	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
\$00	Bank	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$01	Interrupt Ctrl	R	RX_I	TX_I	TM1_I	TM0_I	TBH_I	TBL_I	-	EX_I
		W	RX_IE	TX_IE	TM1_IE	TM0_IE	TBH_IE	TBL_IE	-	EX_IE
\$02	Interrupt Ctrl Clear	R	-	-	-	-	-	-	-	-
		W	RX_IC	TX_IC	TM1_IC	TM0_IC	TBH_IC	TBL_IC	-	EX_IC
\$03	BEX Config	R	-	-	-	-	-	-	-	-
		W	MEXT	-	-	-	-	-	-	-
\$04	CPU Clock Ctrl	R	PWM CK SEL	-	-	-	-	CKS2	CKS1	CKS0
		W	PWM CK SEL	-	-	-	-	CKS2	CKS1	CKS0
\$05	Port A Strobe Pull-high	R	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
		W	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
\$06	Port A Config	R	PCA7	PCA6	PCA5	PCA4	PCA3	PCA2	PCA1	PCA0
		W	PCA7	PCA6	PCA5	PCA4	PCA3	PCA2	PCA1	PCA0
\$07	Port A Dir	R	DIRA7	DIRA6	DIRA5	DIRA4	DIRA3	DIRA2	DIRA1	DIRA0
		W	DIRA7	DIRA6	DIRA5	DIRA4	DIRA3	DIRA2	DIRA1	DIRA0
\$08	Port A Data (Wakeup port)	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$09	Port D Data	R	-	-	b5	b4	b3	b2	b1	b0
		W	-	-	b5	b4	b3	b2	b1	b0
\$0A	Port B Data	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$0B	Port C Data	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	B7	B6	B5	B4	B3	B2	B1/EXC	b0
\$0C	Timebase Sel	R	-	-	-	-	TBL0	TBL1	TBH0	TBH1
		W	-	-	-	-	TBL0	TBL1	TBH0	TBH1
\$0D	BEX Vol. ID	R	-	-	-	-	-	-	-	-
		W	-	-	-	-	-	VID2	VID1	VID0
\$0E	C32K Ctrl	R	-	-	-	-	-	-	-	-
		W	C32KEN	-	-	-	-	-	-	-
\$0F	Timer Ctrl	R	-	TM0C11	TM0C10	TM0C22	TM0C21	TM0C20	TM1S1	TM1S0
		W	-	TM0C11	TM0C10	TM0C22	TM0C21	TM0C20	TM1S1	TM1S0
\$10	TM0 Low byte	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$11	TM0 High byte	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$12	PWM Ctrl0	R	CHE0	SP/T	-	DACL1	DACL0	-	-	-

Address	Function	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
\$12	PWM Ctrl0	W	CHE0	SP/T	-	DACL1	DACL0	-	-	-
\$13	PWM Ch.0 Envelope	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$14	TM1 Low byte	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$15	TM1 High byte	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$16	PWM Ctrl1	R	CHE1	SP/T	-	DACH1	DACH0	-	-	-
		W	CHE1	SP/T	-	DACH1	DACH0	-	-	-
\$17	PWM Ch.1 Envelope	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$18	Wakeup Ctrl	R	-	-	RXW	TM1W	TBHW	TM0W	TBLW	KEYW
		W	-	-	RXEN	TM1EN	TBHEN	TM0EN	TBLEN	KEYEN
\$19	UART Cmd1	R	-	-	-	-	-	-	-	-
		W	RxIntEn	TxIntEn	I_Reset	-	Parity	P_Check	SCLK1	SCLK0
\$1A	UART Cmd2	R	RxRDY	TxRDY	FE	OE	PE	-	-	AcRDY
		W	RxPinEn	TxPinEn	-	-	-	-	-	-
\$1B	UART Data	R	b7	b6	b5	b4	b3	b2	b1	b0
		W	b7	b6	b5	b4	b3	b2	b1	b0
\$1C	Baud Scalar Lo	R	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
		W	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
\$1D	Baud Scalar Hi	R	-	-	-	MB12	MB11	MB10	MB9	MB8
		W	-	-	-	MB12	MB11	MB10	MB9	MB8
\$1E	Baud Rate Lo	R	NB7	NB6	NB5	NB4	NB3	NB2	NB1	NB0
		W	NB7	NB6	NB5	NB4	NB3	NB2	NB1	NB0
\$1F	Baud Rate Hi	R	-	-	-	NB12	NB11	NB10	NB9	NB8
		W	-	-	-	NB12	NB11	NB10	NB9	NB8
\$20	BEX Port0	R	XP0.7	XP0.6	XP0.5	XP0.4	XP0.3	XP0.2	XP0.1	XP0.0
		W	XP0.7	XP0.6	XP0.5	XP0.4	XP0.3	XP0.2	XP0.1	XP0.0
\$21	BEX Port1	R	XP1.7	XP1.6	XP1.5	XP1.4	XP1.3	XP1.2	XP1.1	XP1.0
		W	XP1.7	XP1.6	XP1.5	XP1.4	XP1.3	XP1.2	XP1.1	XP1.0
\$22	BEX Port2	R	XP2.7	XP2.6	XP2.5	XP2.4	XP2.3	XP2.2	XP2.1	XP2.0
		W	XP2.7	XP2.6	XP2.5	XP2.4	XP2.3	XP2.2	XP2.1	XP2.0
\$23	BEX Config	R	-	-	-	-	-	-	-	-
		W	CFG2	CFG1	CFG0	DIR2	DIR1	DIR03	DIR01	DIR00
\$24*	LCD OPT	R	-	DUTY32	BOP1	BOP0	ALL_OFF	ALL_ON	STRBEN	LCDEN
		W	-	DUTY32	BOP1	BOP0	ALL_OFF	ALL_ON	STRBEN	LCDEN
\$25*	Pump Ctrl	R	PUMPEN	-	-	-	DIV1	DIV0	PUMP1	PUMP0
		W	PUMPEN	-	-	-	DIV1	DIV0	PUMP1	PUMP0
\$26*	VLCD Ctrl	R	-	-	-	E4	E3	E2	E1	E0
		W	-	-	-	E4	E3	E2	E1	E0

Address	Function	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
\$27*	Port CD Config	R	-	-	PD1SEL	PD0SEL	PC3SEL	PC2SEL	PC10S1	PC10S0
		W	-	-	PD1SEL	PD0SEL	PC3SEL	PC2SEL	PC10S1	PC10S0
\$28*	Port B Config	R	-	-	-	-	PCB3	PCB2	PCB1	PCB0
		W	-	-	-	-	PCB3	PCB2	PCB1	PCB0
\$29*	Port B Dir	R	-	-	-	-	DIRB3	DIRB2	DIRB1	DIRB0
		W	-	-	-	-	DIRB3	DIRB2	DIRB1	DIRB0
\$2A*	Port C Config	R	PCC7	PCC6	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0
		W	PCC7	PCC6	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0
\$2B*	Port C Dir	R	DIRC7	DIRC6	DIRC5	DIRC4	DIRC3	DIRC2	DIRC1	DIRC0
		W	DIRC7	DIRC6	DIRC5	DIRC4	DIRC3	DIRC2	DIRC1	DIRC0
\$2C*	Port D Config	R	-	-	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
		W	-	-	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
\$2D*	Port D Dir	R	-	-	DIRD5	DIRD4	DIRD3	DIRD2	DIRD1	DIRD0
		W	-	-	DIRD5	DIRD4	DIRD3	DIRD2	DIRD1	DIRD0
\$2E	LCD CTL1	R	Duty1	Duty0	-	VCIB2	VCIB1	VCIB0	Bias1	Bias0
		W	Duty1	Duty0	-	VCIB2	VCIB1	VCIB0	Bias1	Bias0
\$30	Serial SRAM Data	R	D7	D6	D5	D4	D3	D2	D1	D0
		W	D7	D6	D5	D4	D3	D2	D1	D0
\$31	Serial SRAM Addr1	R	M7	M6	M5	M4	M3	M2	M1	M0
		W	M7	M6	M5	M4	M3	M2	M1	M0
\$32	Serial SRAM Addr2	R	M15	M14	M13	M12	M11	M10	M9	M8
		W	M15	M14	M13	M12	M11	M10	M9	M8
\$33	Serial SRAM Addr3	R	M23	M22	M21	M20	M19	M18	M17	M16
		W	M23	M22	M21	M20	M19	M18	M17	M16
\$34	Serial SRAM Ctrl	R	Enable	R/W frame	Send R/W bit	CLKSEL1	CLKSEL0	-	AD_SEL1	AD_SELO
		W	Enable	R/W frame	Send R/W bit	CLKSEL1	CLKSEL0	-	AD_SEL1	AD_SELO
\$35	Serial SRAM Start	R	BUSY	-	-	-	-	-	-	-
		W	-	-	-	-	-	-	-	-
\$36	Serial SRAM Stop	R	-	-	-	-	-	-	-	-
		W	-	-	-	-	-	-	-	-
\$38	NMI Ctrl	R	NMIEN	-	-	-	-	-	TM1_F	LV_F
		W	NMIEN	-	-	-	-	-	TM1_E	LV_E
\$39	LV Ctrl	R	LVDEN	-	LV Status	-	VDSEL	LVSEL2	LVSEL1	LVSELO
		W	LVDEN	-	-	-	VDSEL	LVSEL2	LVSEL1	LVSELO
\$3A	Keyscan Ctrl	R	R1ON	-	-	-	-	-	SCAN1	SCAN0
		W	R1ON	-	-	-	-	-	SCAN1	SCAN0
\$3B	Keyscan Port1	-	-	-	-	-	-	-	-	-
		W	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
\$3C	Keyscan Port2	-	-	-	-	-	-	-	-	-

Address	Function	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
\$3C	Keyscan Port2	W	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
\$3E	Mirror Byte	R	D0	D1	D2	D3	D4	D5	D6	D7
		W	D7	D6	D5	D4	D3	D2	D1	D0
\$3F	Swap Nibble	R	D3	D2	D1	D0	D7	D6	D5	D4
		W	D7	D6	D5	D4	D3	D2	D1	D0
\$3000	SPI TXD0	-	-	-	-	-	-	-	-	-
		W	TDX7	TDX6	TDX5	TDX4	TDX3	TDX2	TDX1	TDX0
\$3001	SPI TXD1	-	-	-	-	-	-	-	-	-
		W	TDX15	TDX14	TDX13	TDX12	TDX11	TDX10	TDX9	TDX8
\$3002	SPI TXD2	-	-	-	-	-	-	-	-	-
		W	TDX23	TDX22	TDX21	TDX20	TDX19	TDX18	TDX17	TDX16
\$3003	SPI TXD3	-	-	-	-	-	-	-	-	-
		W	TDX31	TDX30	TDX29	TDX28	TDX27	TDX26	TDX25	TDX24
\$3004	SPI RXD0	R	RDX7	RDX6	RDX5	RDX4	RDX3	RDX2	RDX1	RDX0
		-	-	-	-	-	-	-	-	-
\$3005	SPI RXD1	R	RDX15	RDX14	RDX13	RDX12	RDX11	RDX10	RDX9	RDX8
		-	-	-	-	-	-	-	-	-
\$3006	SPI RXD2	R	RDX23	RDX22	RDX21	RDX20	RDX19	RDX18	RDX17	RDX16
		-	-	-	-	-	-	-	-	-
\$3007	SPI RXD3	R	RDX31	RDX30	RDX29	RDX28	RDX27	RDX26	RDX25	RDX24
		-	-	-	-	-	-	-	-	-
\$3008	SPI CTL0	R	EN	SS	Countset1	Countset0	-	Clksel2	Clksel1	Clksel0
		W	EN	SS	Countset1	Countset0	-	Clksel2	Clksel1	Clksel0
\$3009	SPI CTL1	R	-	-	-	-	-	-	-	Ready
		-	-	-	-	-	-	-	-	-
\$3031	Watchdog Clr	-	-	-	-	-	-	-	-	-
		W	Write \$55 to clear watchdog timer							
\$3032	LCD CTL2	R	-	-	-	-	b3	b2	b1	b0
		W	-	-	-	-	b3	b2	b1	b0

- \$24 ~ \$2D cannot be read if \$03.7=1 (MEXT =1).

GPLB39B option :

\$3034	Code opt	R	X32KSEL	LVROPT	-	-	-	REGOPT	REGopt1B	REGopt0
		W	X32KSEL	LVROPT	-	-	-	REGOPT	REGopt1B	REGopt0
		initial	0	0	0	0	0	0	0	0

27. Register Reset Value

Address	Power-on reset	Reset pin reset	LVR	Watchdog	Wake-up	LB30	LB31	LB32	LB33	LB34	LB35	LB36	LB37	LB39
\$0	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$1	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$2	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$3	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•		•	•	•			•
\$4	0000 0010	0000 0010	0000 0010	0000 0010	Unchanged	•	•	•	•	•	•	•	•	•
\$5	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•		•	•	•	•	•
\$6	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$7	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$8	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$9	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•					•	
\$0A	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$0B	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$0C	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$0D	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•			•	•	•		•
\$0E	1000 0000	1000 0000	1000 0000	1000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$0F	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$10	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$11	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$12	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$13	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$14	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$15	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•

Address	Power-on reset	Reset pin reset	LVR	Watchdog	Wake-up	LB30	LB31	LB32	LB33	LB34	LB35	LB36	LB37	LB39
\$16	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$17	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$18	0000 0000	0000 0000	0000 0000	0000 0000	See what source wakeup	•	•	•	•	•	•	•	•	•
\$19	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$1A	1100 0000	1100 0000	1100 0000	1100 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$1B	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$1C	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$1D	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$1E	1011 0000	1011 0000	1011 0000	1011 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$1F	0000 0100	0000 0100	0000 0100	0000 0100	Unchanged	•	•	•	•	•	•	•	•	•
\$20	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$21	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$22	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$23	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$24*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$25*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$26*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$27*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$28*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$29*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$2A*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$2B*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$2C*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•

Address	Power-on reset	Reset pin reset	LVR	Watchdog	Wake-up	LB30	LB31	LB32	LB33	LB34	LB35	LB36	LB37	LB39
\$2D*	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•					•	
\$2E	00x0 0000	00x0 0000	00x0 0000	00x0 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$30	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$31	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$32	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$33	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$34	0000 0x00	0000 0x00	0000 0x00	0000 0x00	Unchanged	•	•	•	•	•	•	•	•	•
\$35	0xxx xxxx	0xxx xxxx	0xxx xxxx 0xxx xxxx	0xxx xxxx 0xxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$36	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$38	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$39	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$3A	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$3B	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$3C	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$3E	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$3F	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged	•	•	•	•	•	•	•	•	•
\$3000	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged						•	•		•
\$3001	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged						•	•		•
\$3002	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged						•	•		•
\$3003	xxxx xxxx	xxxx xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxxx xxxx	Unchanged						•	•		•
\$3004	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged						•	•		•
\$3005	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged						•	•		•
\$3006	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged						•	•		•
\$3007	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged						•	•		•

Address	Power-on reset	Reset pin reset	LVR	Watchdog	Wake-up	LB30	LB31	LB32	LB33	LB34	LB35	LB36	LB37	LB39
\$3008	0100 0000	0100 0000	0100 0000	0100 0000	Unchanged						•	•		•
\$3009	xxxx xxx1	xxxx xxx1	xxxx xxx1	xxxx xxx1	Unchanged						•	•		•
\$3030	0000 0000	0000 0000	1000 0000	0100 0000	Unchanged		•		•	•	•	•	•	•
\$3031	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	Unchanged	•	•	•	•	•	•	•	•	•
\$3032	0000 0000	0000 0000	0000 0000	0000 0000	Unchanged					•	•	•		

28. Appendix A. Instruction Set

No	Syntax	Code No.	Code Size	CPU Cycle	Addressing Mode
001	ADC #dd	69H	2	2	immediate
002	ADC aa	65H	2	3	zero page
003	ADC aa,X	75H	2	4	zero page indexed x
004	ADC aaaa	6DH	3	4	absolute
005	ADC aaaa,X	7DH	3	4	absolute indexed x
006	ADC aaaa,Y	79H	3	4	absolute indexed y
007	ADC (aa,X)	61H	2	6	indexed indirect x
008	ADC (aa),Y	71H	2	5	indirect indexed y
009	AND #dd	29H	2	2	immediate
010	AND aa	25H	2	3	zero page
011	AND aa,X	35H	2	4	zero page indexed x
012	AND aaaa	2DH	3	4	absolute
013	AND aaaa,X	3DH	3	4	absolute indexed x
014	AND aaaa,Y	39H	3	4	absolute indexed y
015	AND (aa,X)	21H	2	6	indexed indirect x
016	AND (aa),Y	31H	2	5	indirect indexed y
017	ASL A	0AH	1	2	accumulator
018	ASL aa	06H	2	5	zero page
019	ASL aa,X	16H	2	6	zero page indexed x
020	ASL aaaa	0EH	3	6	absolute
021	ASL aaaa,X	1EH	3	7	absolute indexed x
022	BCC ??	90H	2	2	relative
023	BCS ??	B0H	2	2	relative
024	BEQ ??	F0H	2	2	relative
025	BIT aa	24H	2	3	zero page
026	BIT aaaa	2CH	3	4	absolute
027	BMI ??	30H	2	2	relative
028	BNE ??	D0H	2	2	relative
029	BPL ??	10H	2	2	relative
030	BRK	00H	1	7	implied
031	BVC ??	50H	2	2	relative
032	BVS ??	70H	2	2	relative
033	CLC	18H	1	2	implied
034	CLD	D8H	1	2	implied
035	CLI	58H	1	2	implied
036	CLV	B8H	1	2	implied
037	CMP #dd	C9H	2	2	immediate
038	CMP aa	C5H	2	3	zero page
039	CMP aa,X	D5H	2	4	zero page indexed x
040	CMP aaaa	CDH	3	4	absolute
041	CMP aaaa,X	DDH	3	4	absolute indexed x
042	CMP aaaa,Y	D9H	3	4	absolute indexed y
043	CMP (aa,X)	C1H	2	6	indexed indirect x
044	CMP (aa),Y	D1H	2	5	indirect indexed y
045	CPX #dd	E0H	2	2	immediate
046	CPX aa	E4H	2	3	zero page
047	CPX aaaa	ECH	3	4	absolute
048	CPY #dd	C0H	2	2	immediate
049	CPY aa	C4H	2	3	zero page
050	CPY aaaa	CCH	3	4	absolute
051	DEC aa	C6H	2	5	zero page
052	DEC aa,X	D6H	2	6	zero page indexed x
053	DEC aaaa	CEH	3	6	absolute
054	DEC aaaa,X	DEH	3	7	absolute indexed x
055	DEX	CAH	1	2	implied
056	DEY	88H	1	2	implied

No	Syntax	Code No.	Code Size	CPU Cycle	Addressing Mode
057	EOR #dd	49H	2	2	immediate
058	EOR aa	45H	2	2	zero page
059	EOR aa,X	55H	2	2	zero page indexed x
060	EOR aaaa	4DH	3	3	absolute
061	EOR aaaa,X	5DH	3	3	absolute indexed x
062	EOR aaaa,Y	59H	3	3	absolute indexed y
063	EOR (aa,X)	41H	2	2	indexed indirect x
064	EOR (aa),Y	51H	2	2	indirect indexed y
065	INC aa	E6H	2	5	zero page
066	INC aa,X	F6H	2	6	zero page indexed x
067	INC aaaa	EEH	3	6	absolute
068	INC aaaa,X	FEH	3	7	absolute indexed x
069	INX	E8H	1	2	implied
070	INY	C8H	1	2	implied
071	JMP aaaa	4CH	3	3	absolute
072	JMP (aaaa)	6CH	3	5	indirect absolute
073	JSR aaaa	20H	3	6	absolute
074	LDA #dd	A9H	2	2	immediate
075	LDA aa	A5H	2	3	zero page
076	LDA aa,X	B5H	2	4	zero page indexed x
077	LDA aaaa	ADH	3	4	absolute
078	LDA aaaa,X	BDH	3	4	absolute indexed x
079	LDA aaaa,Y	B9H	3	4	absolute indexed y
080	LDA (aa,X)	A1H	2	6	indexed indirect x
081	LDA (aa),Y	B1H	2	5	indirect indexed y
082	LDX #dd	A2H	2	2	immediate
083	LDX aa	A6H	2	3	zero page
084	LDX aa,Y	B6H	2	4	zero page indexed y
085	LDX aaaa	AEH	3	4	absolute
086	LDX aaaa,Y	BEH	3	4	absolute indexed y
087	LDY #dd	A0H	2	2	immediate
088	LDY aa	A4H	2	3	zero page
089	LDY aa,X	B4H	2	4	zero page indexed x
090	LDY aaaa	ACH	3	4	absolute
091	LDY aaaa,X	BCH	3	4	absolute indexed x
092	LSR A	4AH	1	2	accumulator
093	LSR aa	46H	2	5	zero page
094	LSR aa,X	56H	2	6	zero page indexed x
095	LSR aaaa	4EH	3	6	absolute
096	LSR aaaa,X	5EH	3	7	absolute indexed x
097	NOP	EAH	1	2	implied
098	ORA #dd	09H	2	2	immediate
099	ORA aa	05H	2	3	zero page
100	ORA aa,X	15H	2	4	zero page indexed x
101	ORA aaaa	0DH	3	4	absolute
102	ORA aaaa,X	1DH	3	4	absolute indexed x
103	ORA aaaa,Y	19H	3	4	absolute indexed y
104	ORA (aa,X)	01H	2	6	indexed indirect x
105	ORA (aa),Y	11H	2	5	indirect indexed y
106	PHA	48H	1	3	implied
107	PHP	08H	1	3	implied
108	PLA	68H	1	4	implied
109	PLP	28H	1	4	implied
110	ROL A	2AH	1	2	accumulator
111	ROL aa	26H	2	5	zero page
112	ROL aa,X	36H	2	6	zero page indexed x
113	ROL aaaa	2EH	3	6	absolute
114	ROL aaaa,X	3EH	3	7	absolute indexed x
115	ROR A	6AH	1	2	accumulator
116	ROR aa	66H	2	5	zero page
117	ROR aa,X	76H	2	6	zero page indexed x
118	ROR aaaa	6EH	3	6	absolute

No	Syntax	Code No.	Code Size	CPU Cycle	Addressing Mode
119	ROR aaaa,X	7EH	3	7	absolute indexed x
120	RTI	40H	1	6	implied
121	RTS	60H	1	6	implied
122	SBC #dd	E9H	2	2	immediate
123	SBC aa	E5H	2	3	zero page
124	SBC aa,X	F5H	2	4	zero page indexed x
125	SBC aaaa	EDH	3	4	absolute
126	SBC aaaa,X	FDH	3	4	absolute indexed x
127	SBC aaaa,Y	F9H	3	4	absolute indexed y
128	SBC (aa,X)	E1H	2	6	indexed indirect x
129	SBC (aa),Y	F1H	2	5	indirect indexed y
130	SEC	38H	1	2	implied
131	SED	F8H	1	2	implied
132	SEI	78H	1	2	implied
133	STA aa	85H	2	3	zero page
134	STA aa,X	95H	2	4	zero page indexed x
135	STA aaaa	8DH	3	4	absolute
136	STA aaaa,X	9DH	3	5	absolute indexed x
137	STA aaaa,Y	99H	3	5	absolute indexed y
138	STA (aa,X)	81H	2	6	indexed indirect x
139	STA (aa),Y	91H	2	6	indirect indexed y
140	STX aa	86H	2	3	zero page
141	STX aa,Y	96H	2	4	zero page indexed y
142	STX aaaa	8EH	3	4	absolute
143	STY aa	84H	2	3	zero page
144	STY aa,X	94H	2	4	zero page indexed x
145	STY aaaa	8CH	3	4	absolute
146	TAX	AAH	1	2	implied
147	TAY	A8H	1	2	implied
148	TSX	BAH	1	2	implied
149	TXA	8AH	1	2	implied
150	TXS	9AH	1	2	implied
151	TYA	98H	1	2	implied

29. Appendix C, Pin Description

29.1. GPLB3X Pin Description

Please refer to GPLB3X data sheet for detail pin descriptions.

29.2. EV Chip Pin Description

LB30 EV-chip

PIN Name	Type	Description
SEG73 - SEG0	O	LCD driver segment output. SEG15-0 share pad with key scan port.
COM31 - COM0	O	LCD driver common output.
PA7 - PA0	I/O	Port A is a bi-directional I/O port, can be software programmed as wake up I/O.
PB7 - PB0	I/O	Port B is a bi-directional I/O port. Share pad with Bus Extender Interface Addr/Data.
PC1/MC1/SDA PC0/MC0/SCK	I/O	Port C is a bi-directional I/O port. Share pad with Bus Extender MC1-0. Also share pad with SDA/SCK.
PC3/Rx	I	UART input. Share pad with PC3.
PC2/Tx	O	UART output. Share pad with PC2.
PC7 - PC4	I/O	Port C is a bi-directional I/O port.
PD5 - PD2 PD0/IRTx PD1/IRRx	I/O	Port D is a bi-directional I/O port. PD0 share pad with IRTx. PD1 share pin with IRRx.
ROSC	I	R-oscillator input, connect to VDD through a resistor.
RESETB	I	System reset input, low active.
AUDA AUSB	O	PWM audio output.
ROSC32	I	32768 ROSC input, connect to VDD through a resistor.
X32I	I	32.768KHz crystal input.
X32O	O	32.768KHz crystal output.
TEST	I	Test input.
CUP4-CUP1	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VLCD	P	LCD voltage generation.
V5-V1	P	LCD voltage generation.
VDD	P	Power supply voltage input.
VSS	P	Ground reference.
PVDD	P	PWM driver power.
PVSS	P	PWM driver ground reference.

PIN Name	Type	Description
ICE Interface		
XMA20-XMA15	O	Bank select address.
XA15-XA0	I/O	Address bus.
XDC7-XDC0	I/O	Data bus.
CKINP	I	Internal clock input.
CKOUTP	O	Internal clock output.
XCPUCK	O	External ICE clock output.
CPUEN	I	Internal CPU enable. (high active)
XRWB	I/O	CPU R/W signal. (0: write; 1: read)
XCPURSTB	O	CPU reset signal. (low active)
XNMI	O	CPU NMI signal output. (low active)
XINT	O	CPU INT signal output. (low active)
XROMOEB	O	External ROM OE signal output. (low active)
XSLEEP	O	System sleep status output. (high active)
WDOGEN	I	Enable watchdog. (0:disable; 1:enable)
X32KSEL	I	32768 clock oscillator select. (0:X'tal; 1:R-osc)
SRAMSZ[1:0]	I	Select EMU chip SRAM size. (00:1K; 01:2.5K; 10:4K; 11:8K)
DPRAMSZ	I	Select LCD RAM range. (0:\$3e00-3eff; 1:\$3e00-3fff)
PWMDACSEL	I	Select audio output thru PWM or DAC. (0:DAC; 1:PWM)

Legend: I = Input O = Output P = Power

Total pin count: 208

LB30B EV-chip

PIN Name	Type	Description
SEG73 - SEG0	O	LCD driver segment output. SEG15-0 share pad with key scan port.
COM31 - COM0	O	LCD driver common output.
PA7 - PA0	I/O	Port A is a bi-directional I/O port, can be software programmed as wake up I/O.
PB7 - PB0	I/O	Port B is a bi-directional I/O port. Share pad with Bus Extender Interface Addr/Data
PC1/MC1/SDA PC0/MC0/SCK	I/O	Port C is a bi-directional I/O port. Share pad with Bus Extender MC1-0. Also share pad with SDA/SCK.
PC3/Rx	I	UART input. Share pad with PC3.
PC2/Tx	O	UART output. Share pad with PC2.
PC7 - PC4	I/O	Port C is a bi-directional I/O port.
PD5 - PD2 PD0/IRTx PD1/IRRx	I/O	Port D is a bi-directional I/O port. PD0 share pad with IRTx. PD1 share pin with IRRx.

PIN Name	Type	Description
ROSC	I	R-oscillator input, connect to VDD through a resistor
RESETB	I	System reset input, low active.
AUDA AUSB	O	PWM audio output
ROSC32	I	32768 ROSC input, connect to VDD through a resistor
X32I	I	32.768KHz crystal input
X32O	O	32.768KHz crystal output
CUP4-CUP1	P	LCD voltage generation. Charge pump capacitor interconnection pins
VLCD	P	LCD voltage generation.
V4-V1	P	LCD voltage generation.
VDD	P	Power supply voltage input
VSS	P	Ground reference
PVDD	P	PWM driver power
PVSS	P	PWM driver ground reference
ICE Interface		
XROMCEB	O	External ROM CE signal output(low active)
XMA19-XMA15	O	Bank select address
XA15-XA0	I/O	Address bus
XDC7-XDC0	I/O	Data bus
CKINP	I	Internal clock input
CKOUTP	O	Internal clock output
XCPUCK	O	External ICE clock output
CPUEN	I	Internal CPU enable (high active)
XRWB	I/O	CPU R/W signal (0: write; 1: read)
XCPURSTB	O	CPU reset signal (low active)
XNMIB	O	CPU NMI signal output (low active)
XINTB	O	CPU INT signal output (low active)
XROMOEB	O	External ROM OE signal output(low active)
XSLEEP	O	System sleep status output (high active)
WDOGEN	I	Enable watchdog (0:disable; 1:enable)
X32KSEL	I	32768 clock oscillator select (0:X'tal; 1:R-osc)
BODYOPT[2:0]	I	Select EMU chip body(body select table for detail)
ALONOPTB	I	Bodyopt enable signal(0:enable;1:disable)
REG_OPTP[1:0]	I	Regulator level option(00:2.5V; 01:2.6V; 10:2.7V; 11:3.0V)
REG_ENP	I	Regulator enable signal(0:disable;1:enable)
LVR_ENP	I	LVR enable signal(0:disable;1:enable)
PWMDACSEL	I	Select audio output thru PWM or DAC(0:DAC; 1:PWM)
NEW_EMU	I	Emulation body select(1:new body;0:old body)
VROUT	P	Regulator Voltage output

Legend: I = Input O = Output P = Power

Total pin count: 216

LB35 EV-chip

PIN Name	Type	Description
SEG83 - SEG0	O	LCD driver segment output. SEG15-0 share pad with key scan port.
SEG99/COM32 – SEG84/COM47	O	LCD driver segment/common output.
COM15 - COM0	O	LCD driver common output.
PA7 - PA0	I/O	Port A is a bi-directional I/O port, can be software programmed as wake up I/O.
PB7 - PB0	I/O	Port B is a bi-directional I/O port. Share pad with Bus Extender Interface Addr/Data.
PC1/MC1/SDA PC0/MC0/SCK	I/O	Port C is a bi-directional I/O port. Share pad with Bus Extender MC1-0. Also share pad with SDA/SCK.
PC4	I/O	Port C is a bi-directional I/O port.
PC3/Rx	I	UART input. Share pad with PC3.
PC2/Tx	O	UART output. Share pad with PC2.
ROSC	I	R-oscillator input, connect to VDD through a resistor.
RESETB	I	System reset input, low active.
AUDA AUSB	O	PWM audio output.
ROSC32	I	32768 ROSC input, connect to VDD through a resistor.
X32I	I	32.768KHz crystal input.
X32O	O	32.768KHz crystal output.
CAP1P CAP1N CAP2P CAP2N	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VPP	P	LCD voltage generation.
VCI	P	LCD voltage generation.
VLCD	P	LCD voltage generation.
VROUT	P	Voltage regulator output.
VDD	P	Power supply voltage input.
VSS	P	Ground reference.
PVDD	P	PWM driver power.
PVSS	P	PWM driver ground reference.
ICE Interface		
XMA19-XMA15	O	Bank select address.
XA15-XA0	I/O	Address bus.
XDC7-XDC0	I/O	Data bus.
CKINP	I	Internal clock input.

PIN Name	Type	Description
CKOUTP	O	Internal clock output.
XCPUCK	O	External ICE clock output.
CPUEN	I	Internal CPU enable. (high active)
XRWB	I/O	CPU R/W signal. (0: write; 1: read)
XCPURSTB	O	CPU reset signal. (low active)
XNMI	O	CPU NMI signal output. (low active)
XINT	O	CPU INT signal output. (low active)
XROMOEB	O	External ROM OE signal output. (low active)
XSLEEP	O	System sleep status output. (high active)
XWDOGEN	I	Enable watchdog. (0:disable; 1:enable)
X32KSEL	I	32768 clock oscillator select. (0:X'tal; 1:R-osc)
XREGVOPT[1:0]	I	Voltage regulator output level select.
XREGENBOPT	I	Voltage regulator enable/disable. (0:enable; 1:disable)
XLVREN	I	LVR enable/disable. (0:disable; 1:enable)
XCKFLTEN	I	For Generalplus test only.
DVP	I	For Generalplus test only.
XCODOPT_LB1	I	For Generalplus test only.
NEW_EMU	I	For Generalplus test only.

Legend: I = Input O = Output P = Power

Total pin count: 224

LB39B EV-chip

PIN Name	Type	Description
SEG95 - SEG0	O	LCD driver segment output. SEG15-0 share pad with key scan port.
SEG111/COM63 – SEG96/COM48	O	LCD driver segment/common output.
COM47 – COM0	O	LCD driver common output.
PA7 – PA0	I/O	Port A is a bi-directional I/O port, can be software programmed as wake up I/O.
PB7 – PB0	I/O	Port B is a bi-directional I/O port. Share pad with Bus Extender Interface Addr/Data.
PC1/MC1/SDA PC0/MC0/SCK	I/O	Port C is a bi-directional I/O port. Share pad with Bus Extender MC1-0. Also share pad with SDA/SCK.
PC4	I/O	Port C is a bi-directional I/O port.
PC3/Rx	I	UART input. Share pad with PC3.
PC2/Tx	O	UART output. Share pad with PC2.
ROSC	I	R-oscillator input, connect to VDD through a resistor.
RESETB	I	System reset input, low active.
AUDA AUDB	O	PWM audio output.

PIN Name	Type	Description
ROSC32	I	32768 ROSC input, connect to VDD through a resistor.
X32I	I	32.768KHz crystal input.
X32O	O	32.768KHz crystal output.
CAP1P CAP1N CAP2P CAP2N	P	LCD voltage generation. Charge pump capacitor interconnection pins.
V4CAP V3CAP V2CAP V1CAP	P	LCD voltage generation.
VPP	P	LCD voltage generation.
VCI	P	LCD voltage generation.
VLCD	P	LCD voltage generation.
VROUT	P	Voltage regulator output.
VDD	P	Power supply voltage input.
VSS	P	Ground reference.
PVDD	P	PWM driver power.
PVSS	P	PWM driver ground reference.
ICE Interface		
XMA20-XMA15	O	Bank select address.
XA15-XA0	I/O	Address bus.
XDC7-XDC0	I/O	Data bus.
CKINP	I	Internal clock input.
CKOUTP	O	Internal clock output.
XCPUCK	O	External ICE clock output.
CPUEN	I	Internal CPU enable. (high active)
XRWB	I/O	CPU R/W signal. (0: write; 1: read)
XCPURSTB	O	CPU reset signal. (low active)
XNMI	O	CPU NMI signal output. (low active)
XINT	O	CPU INT signal output. (low active)
XROMOEB	O	External ROM OE signal output. (low active)
XSLEEP	O	System sleep status output. (high active)
XWDOGEN	I	Enable watchdog. (0:disable; 1:enable)
TRIM_V4_IN2 TRIM_V4_IN1 TRIM_V4_IN0 TRIM_VLCD_IN1 TRIM_VLCD_IN0	I	For Generalplus test only.

Legend: I = Input O = Output P = Power

Total pin count: 256

30. Appendix D. Wave-Form

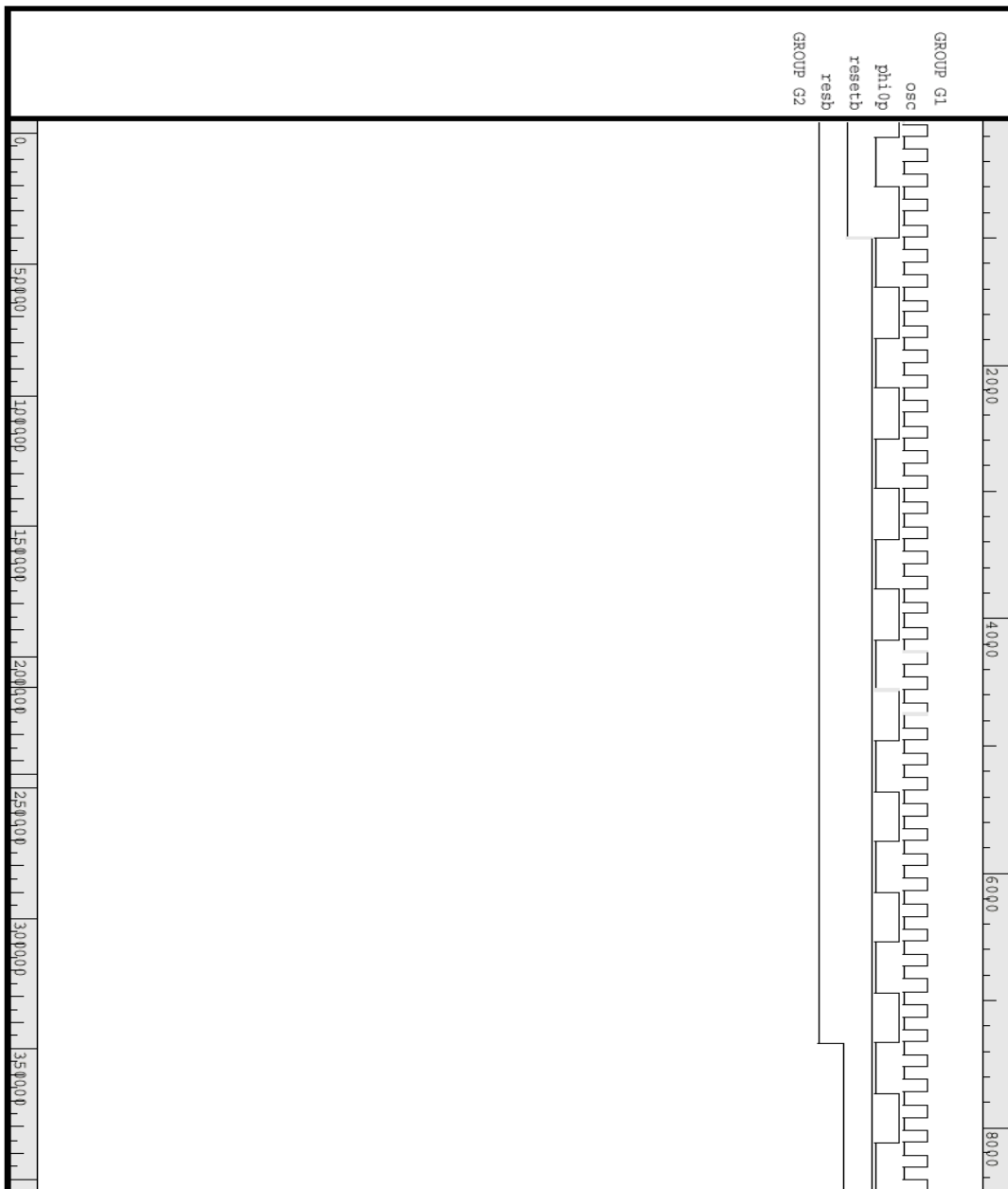
30.1. Reset

$\text{Phi0p} = F_{\text{CPU}} = F_{\text{OSC}} / 4$ (default)

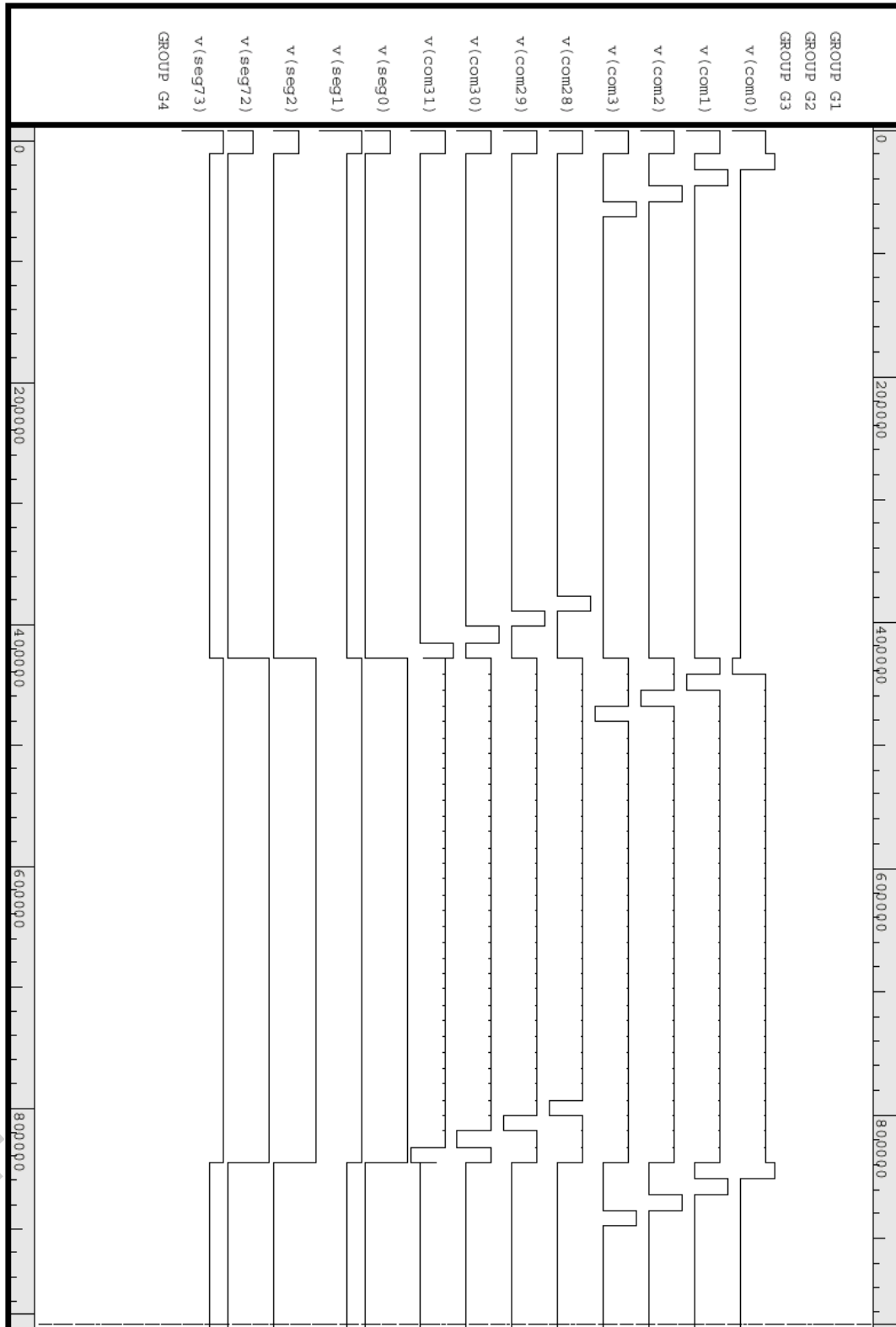
Resetb = reset pin wave form

Resb = IC reset active signal

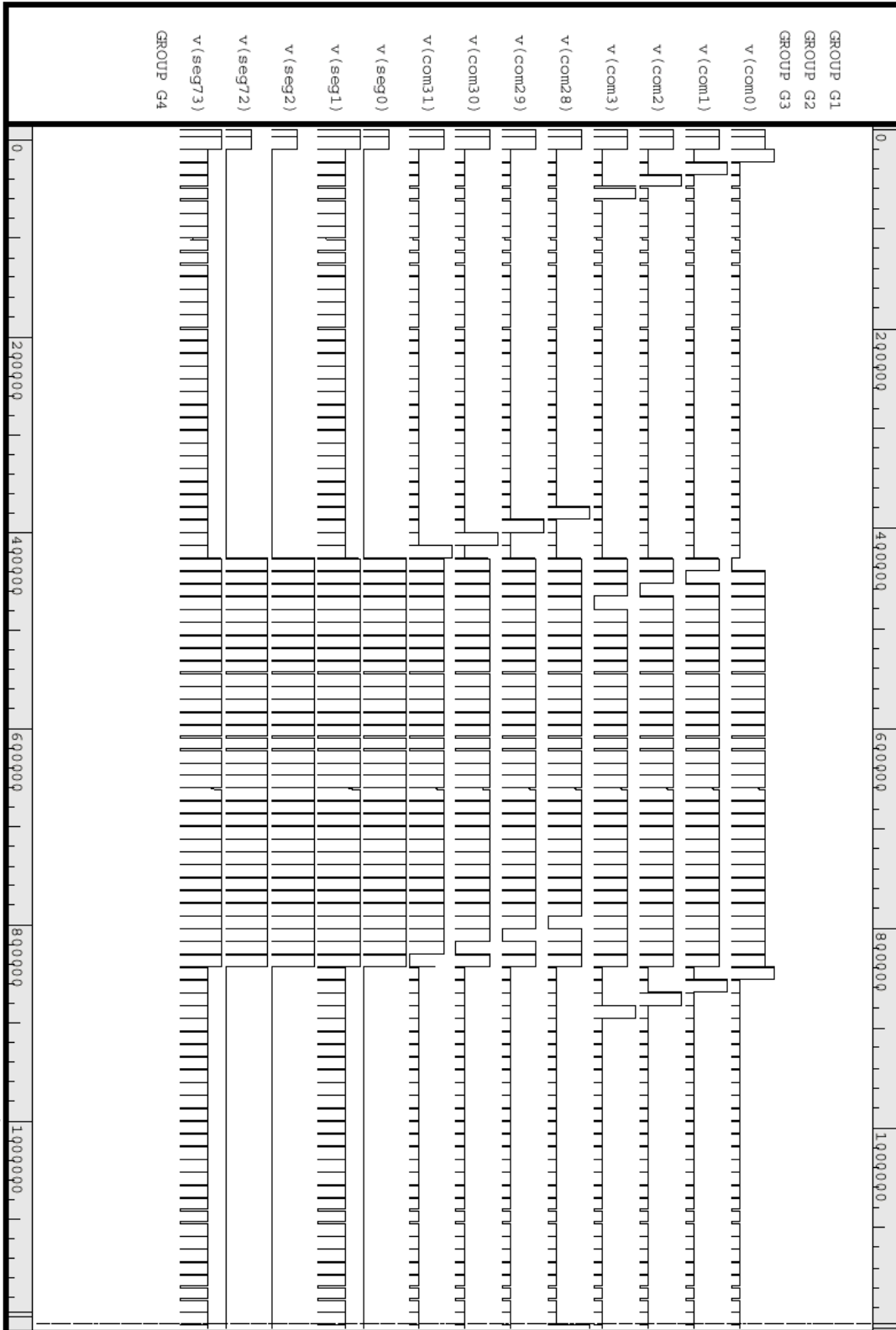
When reset pin releases, CPU reset must delay 8 CPU clock.



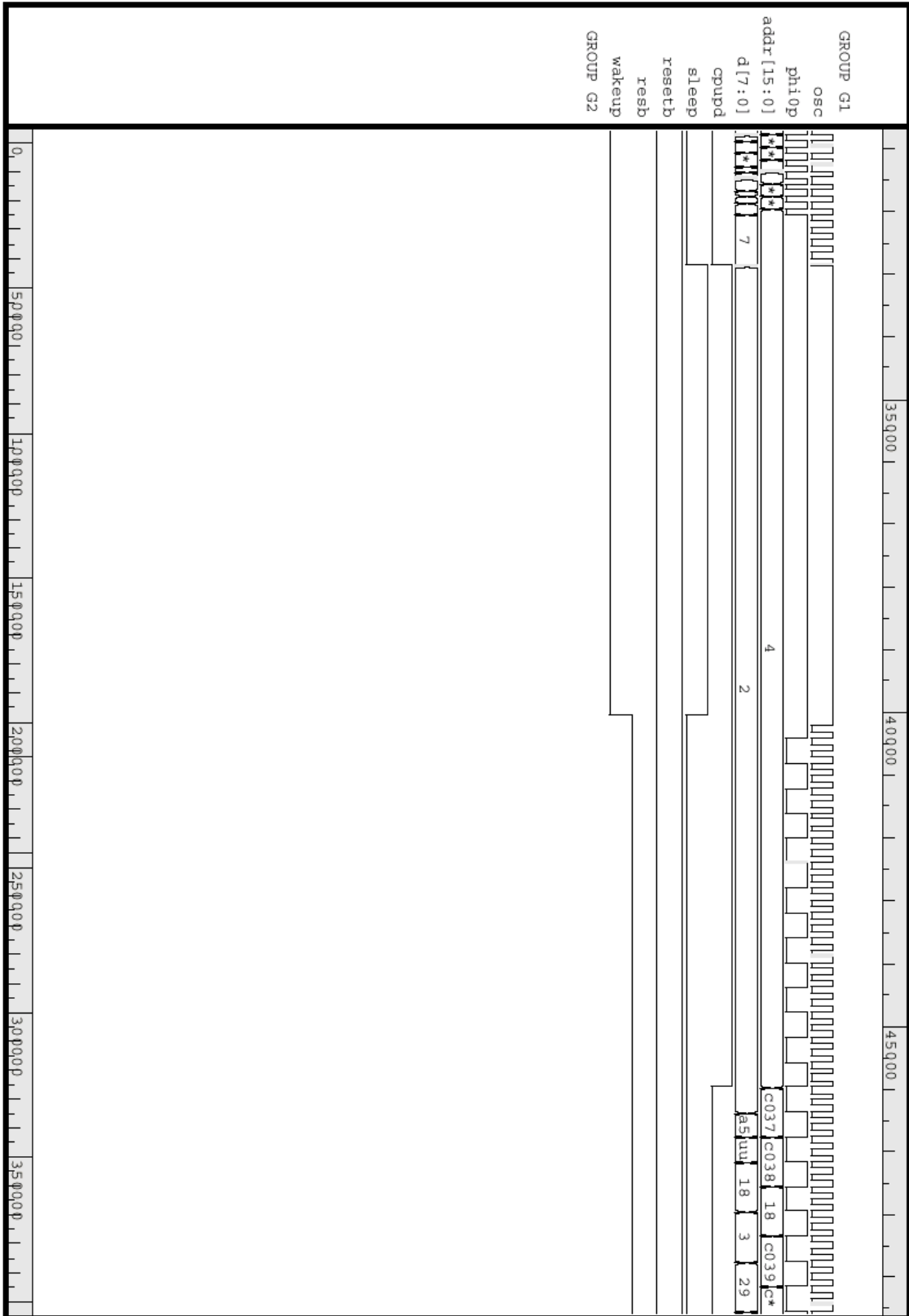
30.2. STRBE-Off-LCD



30.3. STRBE-ON-LCD



30.4. Wake Up



GPLB3X Development System User's Manual

31. Differences between EMU Chip and Real Chip (GPLB32)

31.1. AC/DC Characteristics

Item	Real Chip	Emulation Chip
Operating Voltage	2.4V ~ 3.6V	2.4V ~ 3.6V: if users use some "appropriate" FLASH as internal ROM emulator. "Appropriate" means that FLASH operating voltage is 2.4V ~3.6V and its access time is short enough.
	3.6V ~ 5.5V	3.6V ~ 4.5V: if users use some appropriate FLASH as internal ROM emulator. 4.5V ~ 5.5V: if users use EEPROM/EPROM as internal ROM emulator.
Power Consumption [Operation Current, Halt Mode Current, Standby Current]	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽¹⁾
<ROSC resistor value> vs. <Operating Frequency> Diagram	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽²⁾
I/O Driving Capability	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽³⁾
DAC Current Driving Capability	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽³⁾
PWM Current Driving Capability	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽³⁾
Built-in VLCD Voltage	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽³⁾
LCD Driver Driving Capability	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽³⁾
Low Voltage Reset Voltage Level	Please refer to data sheet for more details	Not guaranteed 100% identical to the real chip ⁽³⁾

- (1) Power consumption of emulation chip's internal-ROM-emulator (external SRAM/ FLASH/ E[E]PROM) is much larger than the real chip's internal mask ROM, and it could be the dominate power consumption of the whole emulation system (ex. piggyback)
- (2) The mask options are replaced by pin options in EV chip. There will be current leakage in EV chip if the pin options are floating. In real chip, the mask options are chosen either VDD or VSS.
- (3) In order to calibrate CPU operating frequency to a desired value, users can use a scope to probe the CPU clock pin [pin #37 of CPU header] on emulation board, and adjust the ROSC resistor according to desired frequency. In addition, if scope or emulation board is not available, there is another way to calibrate CPU operating frequency: writing a software code that makes one I/O-pin to generate a square wave in which clock source is dependent on ROSC frequency.
- (4) It is GENERALPLUS responsibility to assure that the characteristics of each shipping part (real chip IC) are all matched and satisfied with the characteristics depicted on data sheet. However, GENERALPLUS cannot guarantee that the characteristics of emulation chip are 100% identical to the information depicted on data sheet. Therefore, In order to make an accuracy DC/AC characteristics evaluation on IC, its system and interaction with peripheral (ex. LCD display quality, sound volume, I/O driving capability etc), GENERALPLUS strongly recommends customers ordering MOQ for verification.
- (5) Assuring whether CPU is able to enter sleep mode on a piggyback, measurement can be done on ROSC pin. If ROSC is measured at a high level, CPU is in sleep mode. In contrast, if ROSC stays at low level, CPU is in operating mode.

31.2. Hardware Function Characteristics

	Real Chip	Emulation Chip
Pin Assignment	Please refer to data sheet in details	Not identical to the real chip; refer to schematic circuit provided by GENERALPLUS.
Internal ROM	Mask ROM	Emulated by external memory: SRAM / FLASH / E[E]PROM
Internal ROM Access Time	Bellow 100ns	<p>Depends on external emulation memory used by users.</p> <p>Note: Access time of the memory should not be larger than $\frac{1}{\text{operation_Frequency}}$ all the time. For example, if the operation frequency is 5MHz, the access time of external emulation memory should be less than 200ns (1/5MHz).</p> <p>Also, access time depicted on the memory data sheet is under certain operation environment (e.g. operating voltage, data bus loading, etc). In order to assure the timing criterion is matched at all operation conditions and certain timing margin is necessary. For example, if CPU runs at 5MHz, it is much safer to choose the memory in which access time is lower than 150ns (timing margin is 50ns).</p>
32768Hz Clock Source Option <Crystal/ROSC>	Mask Option	Pin Option Floating
Low Voltage Reset Option <EN/DIS>	Mask Option	Pin Option Floating
Watch Dog Option <EN/DIS>	Mask Option	Pin Option Floating
Audio Output Drive Option <PWM/DAC>	Mask Option	Pin Option Floating
PortA[7:6] shared with SEG[62:63] PortB[5:0] shared with SEG [64:69] or COM[6:21] PortC[7:4] shared with SEG[70:73]	Mask Option	I/O, SEG, COM functions are all supported.

	Real Chip	Emulation Chip
or COM[22:25]		
PortC[1:0] shared with SEG[60:61]		
PortD[5:0] shared with COM[26:31]		
(1)		
Go to sleep procedure (2)	may NOT enter sleep mode	Able to enter sleep mode
LDA #00H		
LDX #03H		
LDY #07H		
STA \$05 ;disable key strobe pull function		
STA \$18 ;clear wakeup source		
STX \$18 ;enable wakeup source		
LDA \$08 ;latch wakeup I/O port (portA)		
.....		
.....		
.....		
STY \$04 ;go to sleep		

(1) When an I/O is optional to a LCD segment or common signal, the I/O pin (used as segment or common signal) must be masked off while reading the entire I/O port (8-bit).

(2) Except the instruction of latching wakeup I/O port, DO NOT add any instruction between the instruction <enable wakeup source> and instruction <go to sleep>. Otherwise, real chip may NOT enter sleep mode and make large power consumption.

31.3. Software Function Characteristics

	Real Chip	Emulation Chip
Internal ROM size	Please refer to the section 3.MEMORY MAPPING.	Depends on the size of external emulation memory.
ROM data value which is accessed from the area that is not inside the predefined Internal mask ROM area (ex. the area that exceeds the internal ROM size) *Please note that any intentional or accidental attempt to access, reference (ex. Checksum) or jump/call on this area might cause a serious fail on your really chip. EX. ; Bank Register (\$0=17) exceed ; GPLB32 Rom size LDA #17 STA \$0 LDA #40H LDX #00 STA PAGE0_VAR+1 STX PAGE0_VAR JMP (PAGE0_VAR) ; OR LDA (PAGE0_VAR),X	Random / Unpredictable. Depends on data values that are accessed from the extra area of external emulation memory. If internal ROM emulator is SRAM, these data values may depend on the download procedure of ICE tools or user's ROM emulator< a.k.a. ROMTER>. These data values may be random. If internal ROM emulator is FLASH or E[E]PROM, these data values may depend on the development tools (assembler, linker, binder), or internal program buffer values of FLASH or E[E]PROM writer. Sometimes, if the size of external emulation memory is the same as internal mask ROM, the data value on this exceeding area will be random and unpredictable. Certainly, this is not the same as the data value read on real chip. (1)	
ROM data value which is accessed from test area that is reserved for GENERALPLUS *Please note that any intentional or accidental attempt to access, reference (ex. checksum) or jump/call on this area might cause a	GENERALPLUS Test Program & Test Vector *Please note that GENERALPLUS reserves the right to change test program and test vector without prior notification.	Depends on data values that are accessed from the test area of the external emulation memory. If internal ROM emulator is SRAM, these data values might depend on the download

	Real Chip	Emulation Chip
serious fail on your real chip. EX. ; \$C040 is in test area ; (\$0xC000~0xC7FF). LDA #C0H LDX #40H STA PAGE0_VAR+1 STX PAGE0_VAR JMP (PAGE0_VAR) ; OR LDA (PAGE0_VAR),X		procedure of ICE tools, or the download procedure of ROM emulator (a.k.a. ROMTER). These data values may be random. If internal ROM emulator is FLASH or E[E]PROM, these data values will depend on the development tools (assembler, linker, binder), or internal program buffer values of FLASH/E[E]PROM writer. ^{(2) (3)}
Internal RAM Size	Please refer to the section 3.MEMORY MAPPING.	1216 bytes if [SRAMS1,0] pin option is set to "00".
Internal RAM Area	Please refer to the section 3.MEMORY MAPPING.	0x0040~0x04FF if [SRAMS1,0] pin option is set to "00"
Internal LCD Buffer Size	Please refer to programming guide for more details.	Same if pin option is jumped to "74x32", not "74x16"
Internal LCD Buffer Area	Please refer to programming guide for more details.	Same if pin option is jumped to "74x32", not "74x16"
RAM data value (ex. \$500) which is accessed from the area that is outside from predefined Internal RAM area (\$40 ~ \$4FF) *Please note that any intentional or accidental attempt to access, reference might cause a serious fail on your real chip.	Random/Unpredictable.	Random/Unpredictable. Please note that the data value read on this extra area of emulation chip is not the same as real chip. In addition, the RAM data of this extra area cannot be modified (written) ⁽⁴⁾
Test area [CPU view]	0xC000 ~ 0xC7FF	
Test area [ROM view]	0x4000 ~ 0x47FF	
Test Vector [CPU view]	0xFFFF2 ~ 0xFFFF7	
Test Vector [ROM view]	0x7FF2 ~ 0x7FF7	

- (1) Because the data of FLASH/E[EEPROM] is fixed (cannot be modified) and more predictable (will not be random after power-on) than the SRAM or ROMTER, GENERALPLUS recommends that to verify the final code (not during software development), users have better taken FLASH/E[EEPROM] as internal ROM emulator, rather than using SRAM or ROMTER. In addition, FLASH/ E[EEPROM] is read only, SRAM or ROMTER is readable and modifiable. Operation behavior of FLASH/E[EEPROM] is much similar to the internal mask than SRAM or ROMTER.

- (2) To program ROM code with their FLASH/E[EEPROM] writers, GENERALPLUS recommends that users should use executable binary-file-format (.TSK, .BIN), rather than use some executable vector-description file formats (.S37). This method is to assure that those data values on reserved test area are predefined by development tool (assembler/linker/ binder), so that they are more predictable, and not simply depends on the download/program procedure of FLASH/E[EEPROM] writer.

- (3) GENERALPLUS recommends that users could add "JMP \$" instruction right behind the test area [CPU view], this will help software programmers to investigate any accident jump/call on this test area.

- (4) GENERALPLUS recommends that all the internal SRAM (including LCD buffer) should be initialized to predefined values when IC is powered on at first time. On the other hand, it is software programmers' responsibility to confirm that SRAM value is reliable during the entire IC operation time.

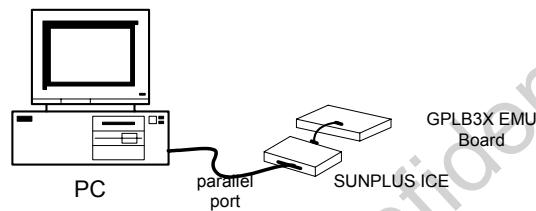
31.4. Application Circuit

	Real Chip	Emulation Chip
Resistor value of ROSC	Please refer to data sheet for more details.	Not guaranteed 100% identical to real chip
Capacitance value that stable 32768 Crystal	Please refer to data sheet for more details.	Not guaranteed 100% identical to real chip

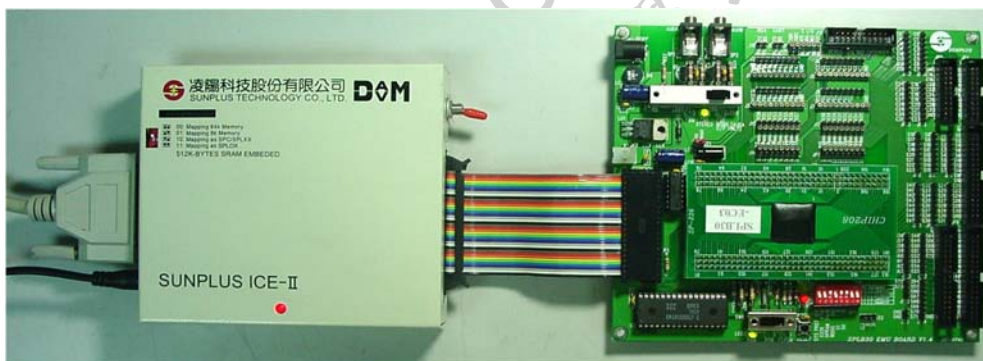
32. EMU Board & Piggy Back

32.1. EMU Board Connection

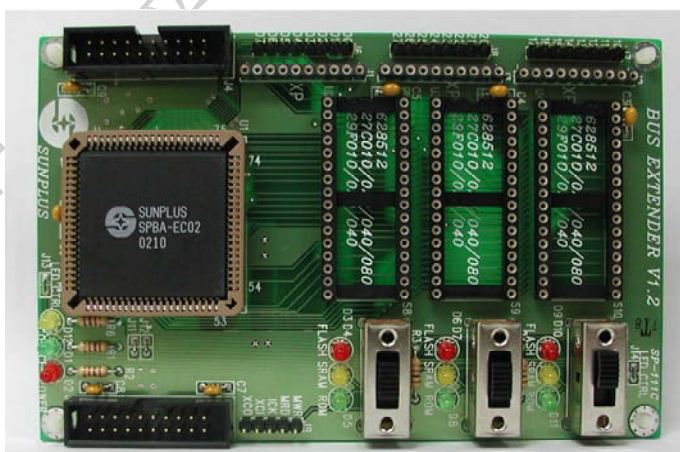
The GPLB30 EMU Board is a shared board for GPLB30/31/32/33A/33B/37. The GPLB35 EMU Board is a shared board for GPLB34/35/36. The GPLB39 EMU Board is a shared board for GPLB39A/39B. Programmer can easily emulate these devices on board. Simply apply the following connection to start developing your project. Make sure power is properly supplied to both ICE and EMU board.



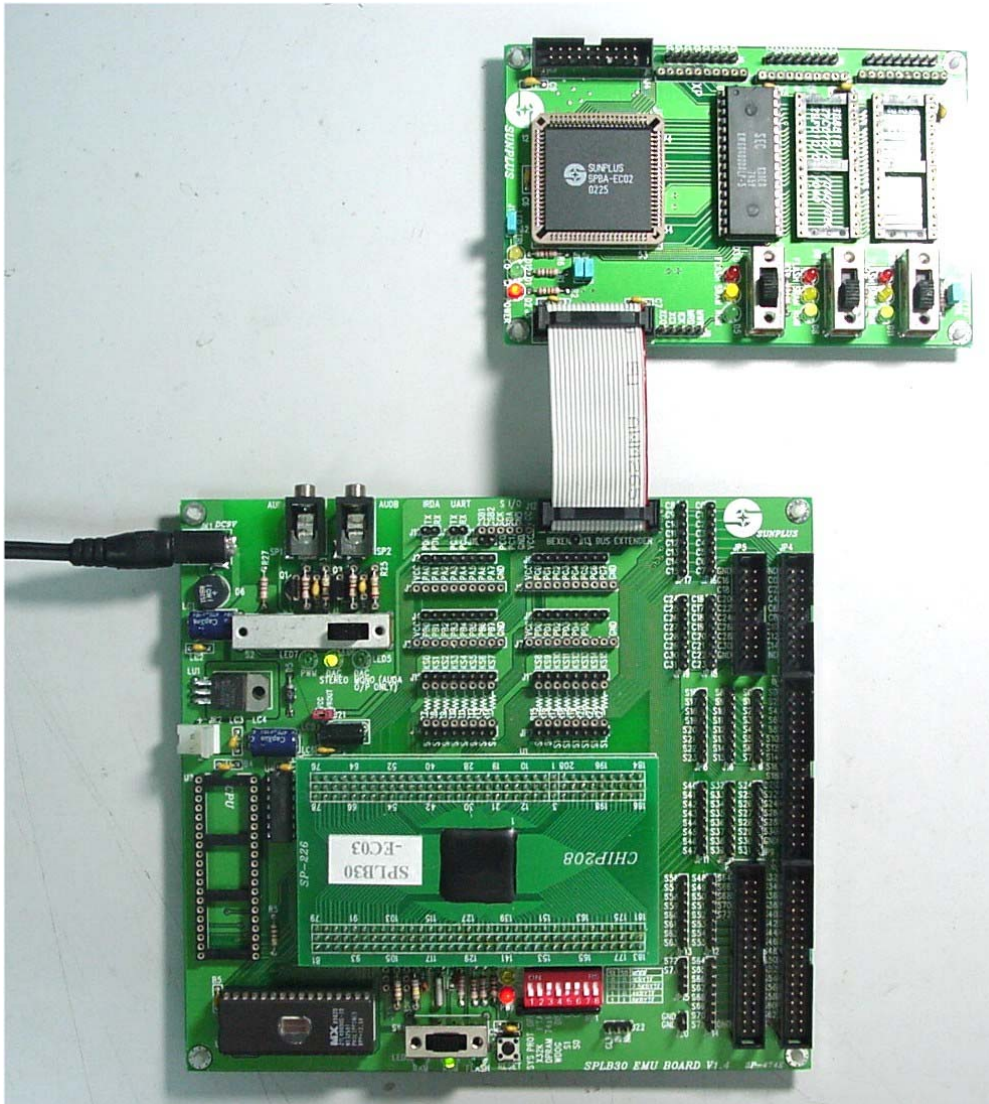
Hardware overview of GPLB3X EMU board + GENERALPLUS ICE



GPBA BUS EXT. board



Hardware overview of GPLB3X EMU board + GPBA BUS EXT board



32.2. GPLB3X Development Component List

Hardware

1. GPLB3X EMU board = GPLB30 /GPLB30B /GPLB35 /GPLB39 EMU board.
2. GPLB30 EMU board V1.4 or earlier: please refer to **GPLB3X Development Board User Manual v1.0** for more details.
3. GPLB30 EMU board V2.1: please refer to **GPLB30B DEV User Manual v1.0** for more details.
4. GPLB35 EMU board: please refer to **GPLB34/GPLB35 EV Board User's Guide v1.0** for more details.
5. GPLB39 EMU board : please refer to **GPLB39 EV Board User's Guide v1.0** for more details.
6. Parallel connector (connects ICE & GPLB3X EMU board).
7. GENERALPLUS ICE (In-Circuit Emulator; sold separately).
8. GPBA BUS EXTENDER BOARD (if necessary).
9. Parallel port (connects to your personal computer; not included in the development kit).
10. Power supplier or adapter with 5V output (not included in the development kit).

Software

1. 6502 assembler and linker¹ (by 2500AD Software Inc.)
2. BinBind.exe (a resource binder by GENERALPLUS), Please refer to **GPDC/GPL13X Binder User Guide v1.0** for more details.

¹ To purchase 6502 assembler and linker, please contact 2500AD Software Inc for details.

32.3. LB3X EV Chip List

	Working Voltage	Max speed	Rom (external)	Ram	I/O			LCD RAM range	LCD comXseg	LCD				Wakeup source	Interrupt source	UART	Serial sram interface	SPI memory interface	Voltage regulator	PWM/DAC	LVR LVD	16Bit Timer	32k WDOG osc
					PA	PB	PC			PD	Vlcd	Bias	Duty										
LB30 EV Chip	2.4-5.5	4MHz	1MB	8128B	8	8	8	6	32*74	32*74	1/5, 1/6	1/16, 1/32	64Hz	6	7	V	V	V	V	V	V	V	V
LB30B EV Chip	2.4-5.5	5MHz	1MB	4288B	8	8	8	6	32*74	32*74	1/3, 1/4, 1/5, 1/6	1/4, 1/8, 1/16, 1/32	64Hz, 68Hz, 73Hz, 79Hz	6	7	V	V	V	V	V	V	V	V
LB35 EV Chip	2.4-5.5	4MHz	2MB	2816B	8	8	5	6	48*100	48*100	1/5, 1/6, 1/7, 1/8	1/16~1/48	64Hz	6	7	V	V	V	V	V	V	V	V
LB39 EV Chip	2.4-5.5	4MHz	2MB	8128B	8	8	5	6	64*112	64*112	1/4, 1/5, 1/6, 1/7, 1/8, 1/9	1/8~1/64	64Hz	6	7	V	V	V	V	V	V	V	V

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