DATA SHEET

凌陽科技
SUNPLUS

SPL130A

128K-byte LCD Controller

OCT. 04, 2001

Version 1.2

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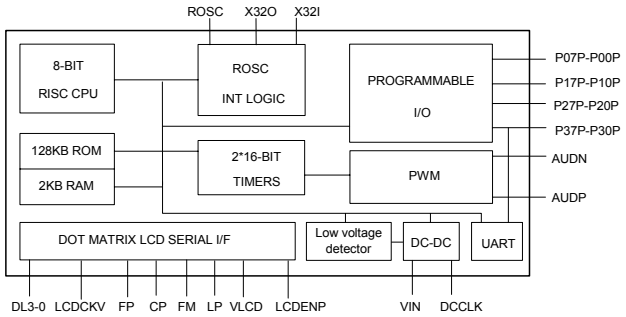
128K-BYTE LCD CONTROLLER

1. GENERAL DESCRIPTION

The SPL130A, an 8-bit microprocessor with advanced CMOS technology, offers a wild assortment of features, including a large size of RAM and ROM, I/Os, PWM audio output, UART, low voltage detector and plus many others. The amount of 128K-byte of ROM and 2K-byte of RAM offer lots of room to store plenty of data and program. Up to 6.0MHz running speed ensures the sophisticated functions and graphics are performed in a flawless way. The 32 programmable I/Os arise the abilities in driving and communicating with other components. The built-in UART facilitates the data communication between devices. In addition, the low voltage detector reports a battery status that gives a clear signal of when to change the battery. The SPL130A includes two sets of 16-bit TIMER/COUNTER circuit that can be programmed as two independent timers, or a 32-bit timer. Furthermore, LCD interface structure can be programmed to implement varieties of dot matrix panel applications from 48*32 to 160*80 with single or more LCD drivers. Other impressed features such as external interrupt sources, sleep mode, key wakeup capability, and E.L driver make SPL130A ranked the best cost and performance ratio in the LCD-controller industry. With fully loads of SUNPLUS state-of-the-art technology and commitment, users are guaranteed to receive completed and satisfactory support.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit RISC controller
- Working Voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Working frequency: 4.0MHz @ 2.4V, 6.0MHz @ 3.6V
- ROM size: 128K bytes
- SRAM size: 2K bytes
- 32 general I/O pins
- Built-in RC Oscillator
- Two channels speech/tone generator
- 8-bit PWM output
- UART receiver and transmitter
- Low voltage detector (2.4V, 2.6V)
- Bus Extender interface for external memory
- Eight interrupt sources
- Two 16-bit Timer/Counter, can cascade to 32-bit timer
- Internal time base generator
- Built-in LCD controller, serially interface with external LCD driver, to drive large dot matrix LCD panel
- Built-in 32768Hz crystal Oscillator
- Low standby current (< 1μA) at power down mode (stop RC oscillator; stop 32768Hz crystal oscillator)
- Wake-up source: key change, Timer0, Timer base

4. APPLICATION FIELD

- Data Bank
- LCD toy/game
- Educational computer
- Consumer, Industry LCD controller

5. SIGNAL DESCRIPTIONS

P: PORT

Mnemonic	PIN No.	Type	Description
P07P - P03P P02P - P00P	15 - 19 21 - 23	I/O	**General I/O** Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both.
P17P - P10P	7 - 14	I/O	**General I/O, key wake up capability.** Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both.
P27P - P20P	47 - 40	I/O	**General I/O /Address/Data Mux IO** Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both.
P37P - P30P	56 - 49	I/O	**General I/O** Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both. **Additional Function** P30P/ EXTI: External interrupt pin P31P/ MC0: Memory interface control signal pin P32P/ECLK: External clock input pin for Timer0 P33P/E.Ldrv0/TO0out: E. L. driver0. When Timer0 overflows, output signals to this pin P34P/E.Ldrv1/TO1out: E. L. driver1. When Timer1 overflows, output signals to this pin. P35P/TX (UART Transmitter): Baud rate ranged from 1200bps to 115.2Kbps. P36P/MC1 (Memory control): Memory interface control signal pin. P37P/RX (UART Receiver)
ROSC	24	I	R-osc input, connect to VDD through a resistor.
RESET	48	I	System reset input pin. Internal pull high. Low active. (see RESET)
AUDP	5	O	PWM Audio output
AUDN	3	O	PWM Audio output
X32I	28	I	32.768KHz crystal input (20p capacitor required)
X32O	27	O	32.768KHz crystal output (20p capacitor required)
TEST1 TEST2	57 1	I I	Test input. Normally floating
VDD	26	I	Digital power input
VSS	6, 20	I	Digital Ground input
DL3 DL2 DL1 DL0	31 32 33 34	O	1-bit LCD data output (DL3), or 4-bit LCD data output (DL3 - 0). *See **"6.7 LCD Interface"***
LCDENP	29	O	LCD enable signal. See ***"6.7 LCD Interface"***
AVDD	4	I	PWM power input
AVSS	2	I	PWM ground input
CPOUT	30	O	LCD data shift clock. See ***"6.7 LCD Interface"***
FM	36	O	LCD alternate signal. See ***"6.7 LCD Interface"***
LP	37	O	LCD data load. See ***"6.7 LCD Interface"***

Mnemonic	PIN No.	Type	Description
FP	35	O	LCD FRAME pulse. See ***"6.7 LCD Interface"***
VIN	25	I	DC-DC input to compare with reference voltage. See ***"6.4 DC_DC LCD Driver"***
DCCLK	58	O	DC-DC charge pump clock. See ***"6.4 DC_DC LCD Driver"***
LCDCKV	38	O	Charge pump clock for SPLD80, SPLD112. See ***"6.7 LCD Interface"***
VLCD	39	I	DC-DC output voltage to supply power for LCD driver (SPLD80 or SPLD112). See ***"6.4 DC_DC LCD Driver"***

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPL130A is an 8-bit CPU, capable of running at highest speed of 6.0MHz. The instruction set is 6502 compatible which involves A, X and Y registers.

6.2. Memory

The SPL130A builds 128K bytes of ROM and 2K bytes of RAM inside the device. In addition, the memory expands as the demand increases. Working with Sunplus bus extender, SPBA01A, to expand RAM or ROM up to 4M bytes.

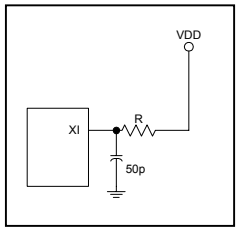
- RAM: 2K bytes
- ROM: 128K bytes, 32KB/bank
- EXTERNAL MEMORY: Using PORT2.0 - PORT2.7, PORT3.1 and PORT3.6, (total of 10 pins) to extend ROM or RAM capacity.

6.3. Clock, Power Mode, LVD/Power Down

6.3.1. Clock

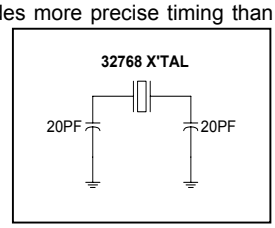
6.3.1.1. System clock

One clock source available: R oscillator. The unique design of R oscillator provides higher frequency and has less effect to the power deviation than other ordinary R-oscillators. The system clock can be used as the sources of timers and UART.



6.3.1.2. 32768 RTC

Two types of RTC available: X'TAL and ROSC (from System Clock source). The 32768Hz X'TAL provides more precise timing than ROSC does. The X'TAL type is highly recommended. The 32768Hz RTC is the source of time-base, TBL and TBH. The time-base can be used for interrupt, wake-up source, timer/counter clock and watchdog timer.



TBL: 2Hz, 4Hz, 8Hz, 16Hz
TBH: 128Hz, 256Hz, 512Hz, 1KHz

6.3.2. Power mode

Three power modes available: Operating, Halt and Standby. A summary depicts the major differences between the three modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz OSC.	ON	ON	OFF
LCD Driver	ON	OFF	OFF

6.3.2.1. Operating mode

In operating state, all functions including CPU, R-oscillator, timer/counter, and LCD controllers are activated.

6.3.2.2. Halt mode

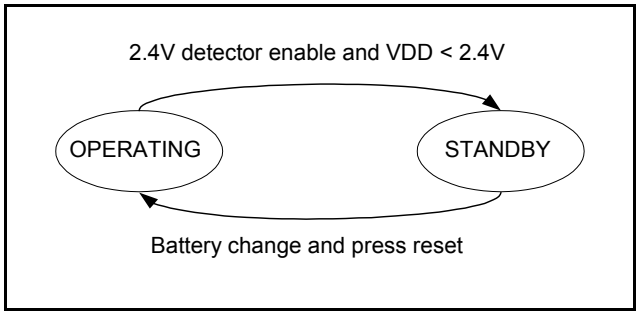
Users have to set TBLEN first and then set CPU clock control CKS2 - CKS0 (in Register $04) to "111" to enter halt state. During halt mode, the 32768Hz oscillator must be enabled to generate time-base wakeup. In addition, users can also enable the key wakeup source for extra wakeup source.

6.3.2.3. Standby mode

To enter standby mode, set CKS2 - CKS0 = "111". The key wake-up is the only wake-up source for returning to the operating mode which means users have to enable key wakeup (b0 in Register $18) before entering standby. In standing-by, all functions are shut down, and RAM and I/O remain in their previous states. The current consumption is minimized in standby mode. If any wakeup event occurs during the halt or standby mode, the first instruction to be executed will be the one after halt or standby instruction.

6.3.3. Low voltage detect/Power down

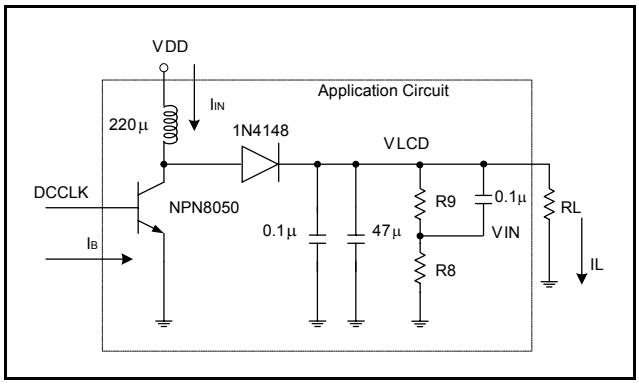
The SPL130A includes a 2.6V/2.4V voltage detector to detect a low voltage event. Users can turn 2.6V detector on and read b6 of Register $18 periodically or enable NMI to monitor if VDD drops below 2.6V. In addition, if 2.4V detector is turned on and VDD does drop below 2.4V, system will shut down all activities automatically and enters standby mode to reduce power consumption. User can use this feature to implement low battery check/battery change function.



State Diagram of Low Voltage Power Down

6.4. DC_DC LCD Driver

Generally, the DC_DC is applied to LCD drivers such as SPLD80, or SPLD112 for charge pump source. The DC-DC circuit in SPL130A generates a supply voltage that is stable and independent to the battery voltage for LCD driver. Its application circuit is shown in following figure. Users can also use a regulator instead and connect the VLCD pin to the output of regulator. The DCCLK generates charge pump clock of DC_DC. A recommended frequency range is from 80KHz through 100KHz. If the frequency is given too slow, the supply voltage will have large ripple. On the other hand, if the frequency is too fast, the charge pump circuit will reduce its efficiency. The DCCLK frequency can be determined by programming Register $32, which forms different brightness for LCD panel. The ratio of the resistors, R9 and R8, influences the DC-DC pump voltage. If the ratio is large, the pump voltage will also be larger. It's also suggested having the value of VLCD larger than VDD; therefore, VLCD will have less effective to VDD variation.



6.5. Interrupt

6.5.1. Interrupt type

Two types of interrupt available: IRQ and NMI

6.5.1.1. IRQ

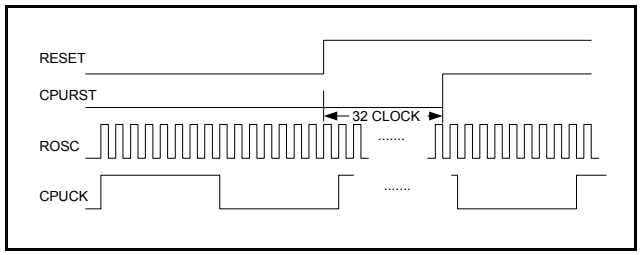
Sources are UART receiver and transmitter, Timer0, Timer1, Time-base TBL and TBH, frame pulse interrupt, and external interrupt.

6.5.1.2. NMI

When working voltage drops below 2.6V, NMI generated and interrupts the CPU.

6.5.2. RESET

When reset pin receives a low signal, the control registers are initialized, but the data stored in SRAM will not be changed. Because there is a pull-high resistor connected to reset pin, a 0.1µF capacitor is required to connect with GND.



6.5.3. Interrupt vector

User Program:

FFFA	NMI
FFFC	RESET
FFFE	IRQ

Test Program:

FFF2	NMI
FFF4	RESET
FFF6	IRQ

6.6. I/O

Four 8-bit I/O ports are available, PORT0 - PORT3. Each of them can be programmed individually to pure output buffer, open drain PMOS (ODP), Open Drain NMOS (ODN), pure input buffer, input with pull-low or pull-high. The individual IO port also has alternative functions. PORT1 has the wakeup capability. The b1 and b6 of PORT3 and PORT2 can be connected to SPBA01 (BUS Extender) to extend RAM or ROM capacity. The b5 and b7 of PORT3 can be used as UART transmitting output and receiving input; besides, b0 can be external interrupt and b2 can be connected to external clock for the clock source of Timer0.

6.6.1. I/O configuration

6.6.1.1. State after reset

PORT0, PORT1, PORT2 and PORT3 are all input mode with pull low state after RESET.

6.6.1.2. I/O port operation

Input Mode:

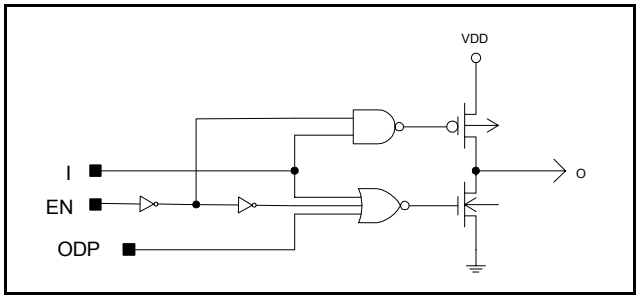
Pure
Pull-high
Pull-low

Output Mode:

Pure
ODP (Open drain PMOS)
ODN (Open drain NMOS)

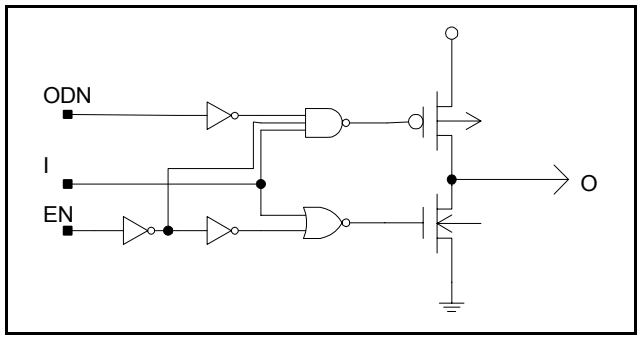
I/O Structure of the state

1). Output Mode with ODP State



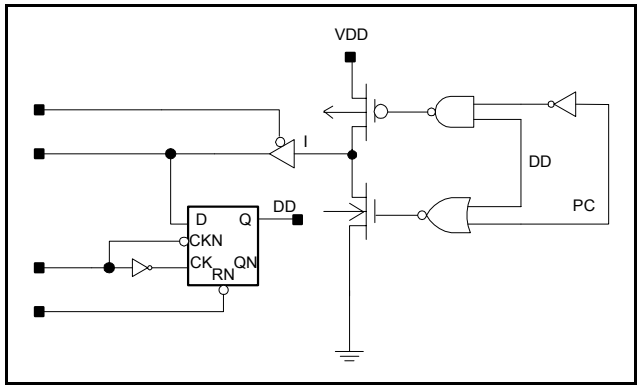
When ODP = H, Output is Open Drain PMOS state
When ODP = L, Output is Pure Output state

2). Output mode with ODN state



When ODN = H, Output is Open Drain NMOS.
When ODN = L, Output is Pure Output.

3). Input Mode with pure, pull high/low states



When PC = H, input is pure state.
When PC = L, input is pull high if DD = H
When PC = L, input is pull low if DD = L

6.7. LCD Interface

6.7.1. LCD controller feature

The built-in LCD controller supports 1-bit or 4-bit data for LCD driver. The LCD data shift clock and frame rate can be programmed according to the amount of data to be displayed on LCD panel and can save more power. The RAM size in SPL130A is 2K bytes. User can determine the size of LCD RAM by giving a start-address and end-address to the configuration port. After the LCD RAM is determined, users have to specify the number of segments in PORT$0E. When the above configurations are completed, the number of commons is determined automatically by hardware. Note that the LCD controller cannot support signals for LCD display while in halt or standby mode.

6.7.2. LCD controller signals

SPL130A provides the following signals for 1-bit LCD driver (e.g. SPLD80, SPLD802, SPLD112) or 4-bit LCD driver (e.g. SPLC206): FM, LP, CPout, DL3 - 0, FP, LCDENP, LCDCKV.

6.7.2.1. FM

The LCD alternate crystal direction output signal is toggled to alternate the crystal polarization on the panel.

6.7.2.2. LP

The LCD line pulse signal is used to latch a line of shifted data onto an LCD panel.

6.7.2.3. CPout

The LCD shift clock signal is the clock output to which the output data to the LCD panel is synchronized.

6.7.2.4. DL3 - 0

The LCD data bus lines transfer pixel data to the LCD panel so that it can be displayed. DL3 is for 1-bit data transferring. DL3 - 0 are for 4-bit data transferring.

6.7.2.5. FP

The LCD frame pulse signal indicates the start of a new display frame.

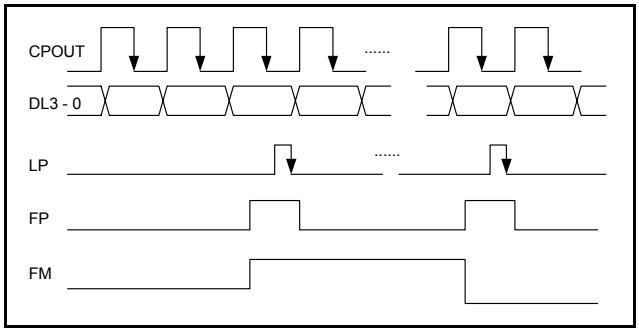
6.7.2.6. LCDENP

LCD enable signal

6.7.2.7. LCDCKV

Charge pump clock for LCD driver, e.g. SPLD80, SPLD112.

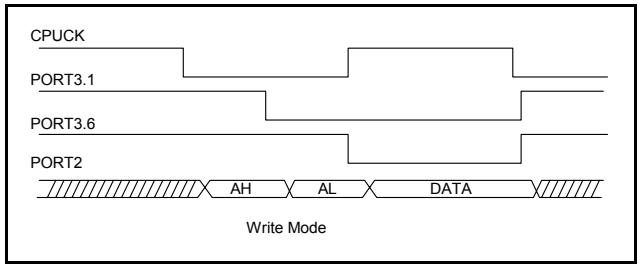
6.7.3. LCD controller signal timing diagram

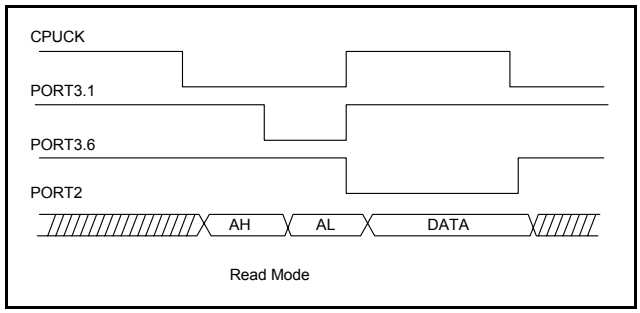


6.8. Bus Interface

The bus interface is a bridge between SPL130A and SPLB01A. The interface is accomplished by PORT2, PORT3.1, and PORT3.6. The PORT3.1 and PORT3.6 are the control signals for PORT2 which can be three states while communicating with SPLB01A: Address High-Byte (AH), Address-Low-Byte (AL) and 8-bit data.

The following diagrams describe the timing relations between control signals, AH, AL and data.





6.9. UART

SPL130A includes 1-channel UART for serial communications. The bit rate ranges as low as from 1200bps and up to 115.2kbps. UART operations are controlled by UART Command Port, $19, and $1A. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be set in Command Port. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt generated when a byte is received or transmitted. By reading the Status Port, $1A, users know whether the interrupt is generated by Rx or Tx. Framing, overrun and parity errors are detected as each byte is received. All error statuses can be read from Status Port, $1A.

The UART supports auto clock calibration. If the auto clock calibration is selected, the standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to Baud Rate Control Ports, $1E and $1F. The supported standard baud rates and their minimum R-oscillator clock frequency are shown in the following table.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto clock calibration is not selected, users can get desired baud rates by writing appropriate values to Pre-scalar Ports, $1C and $1D. Non-standard baud rates can be obtained from this method. When using non-calibration mode, users should aware of the frequency of R-oscillator may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.10. TIMTER

SPL130A provides two 16-bit times, TM0 and TM1, which can be programmed as two independent timers or cascaded to a single 32-bit timer. TM0 can be used as either timer or counter whereas TM1 can only be a timer. The timer's time base is selected from 2Hz up to R-oscillator's clock. For more information, refer to the SPL130A Programming Guide.

6.11. PWM

6.11.1. PWM output

SPL130A contains one pair of PWM outputs supporting with two sound channels. Each channel can play speech or tone individually. SPL130A uses Pulse Width Modulation that could directly drive speaker or buzzer without any buffer or amplification circuit.

6.11.2. Speech and melody

For speech synthesis, SPL130A provides several timer interrupts to make sample frequency more precisely. Users can record or synthesize the sound and digitize it into ROM. After that, the sound can be played back. Two algorithms are recommended for high fidelity and good compression of sound: PCM and ADPCM. PCM provides higher quality of speech but less speech length. ADPCM, on the other hand, offers less quality but longer speech length.

For melody synthesis, SPL130A provides dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically

6.12. Mask Option Summary

6.12.1. WatchDog

The watchdog timer is especially designed for recovering the system from abnormal operation. The watchdog generates a reset signal every one second. Therefore, it must be cleared within one second, 0.5 second is recommended normally. The watchdog works only when the 32768Hz OSC is enabled and read PORT$02 to clear watchdog.

7. ELECTRICAL SPECIFICATIONS

7.1. ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

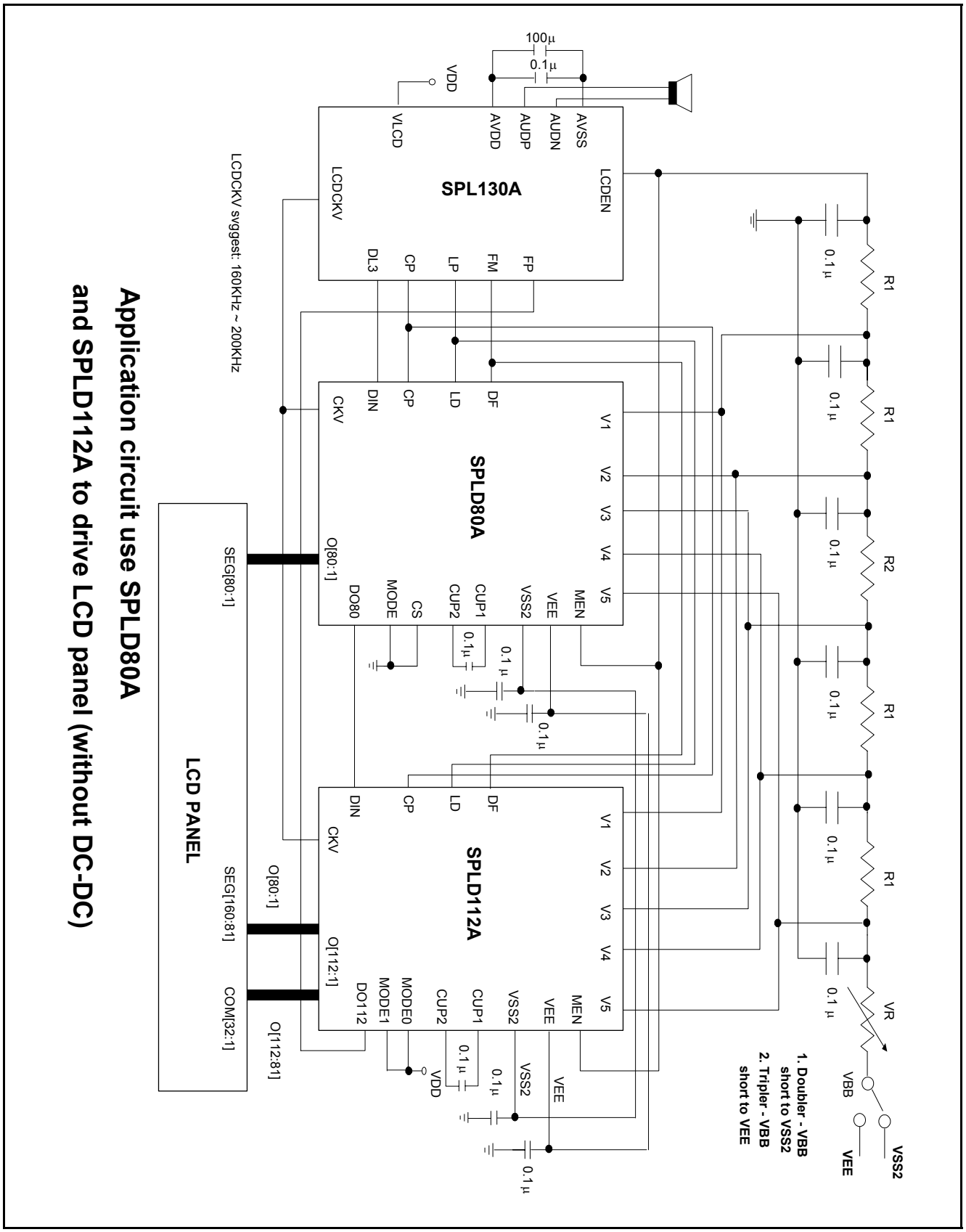
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics

Characteristics	Symbol	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{CC}	-	-	1.0	mA/MHz	VDD = 3.0V
		-	-	2.0	mA/MHz	VDD = 5.0V
Standby Current	I_{STBY}	-	-	1.0	μA	All OSC stop, 32768Hz OFF
Output High I (I/O)	I_{OH}	-	3.0	-	mA	VDD = 5.0V, V_{OH} = 4.2V
	I_{OH}	-	2.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (I/O)	I_{OL}	-	2.0	-	mA	VDD = 5.0V, V_{OL} = 0.8V
	I_{OL}	-	1.0	-	mA	VDD = 3.0V, V_{OL} = 0.8V
CPU Frequency	F_{CPU}	0.1	-	4.0	MHz	VDD = 2.4V
		0.1	-	6.0	MHz	VDD = 3.6V
PWM Drive Current	I_{POH}	-	100	-	mA	VDD = 5.0V, V_{OH} = 3.3V
PWM Sink Current	I_{POL}	-	110	-	mA	VDD = 5.0V, V_{OL} = 1.67V

8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)



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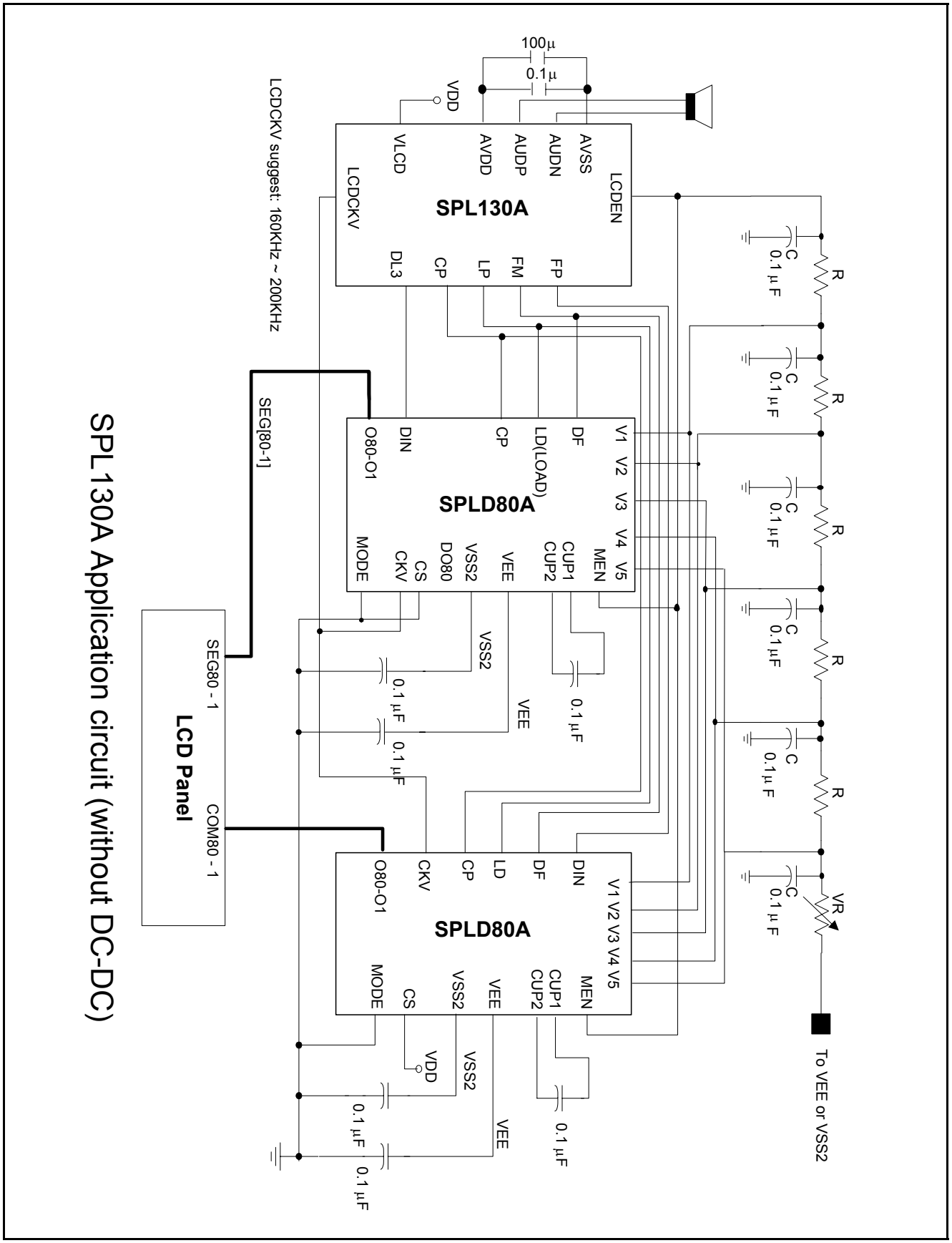
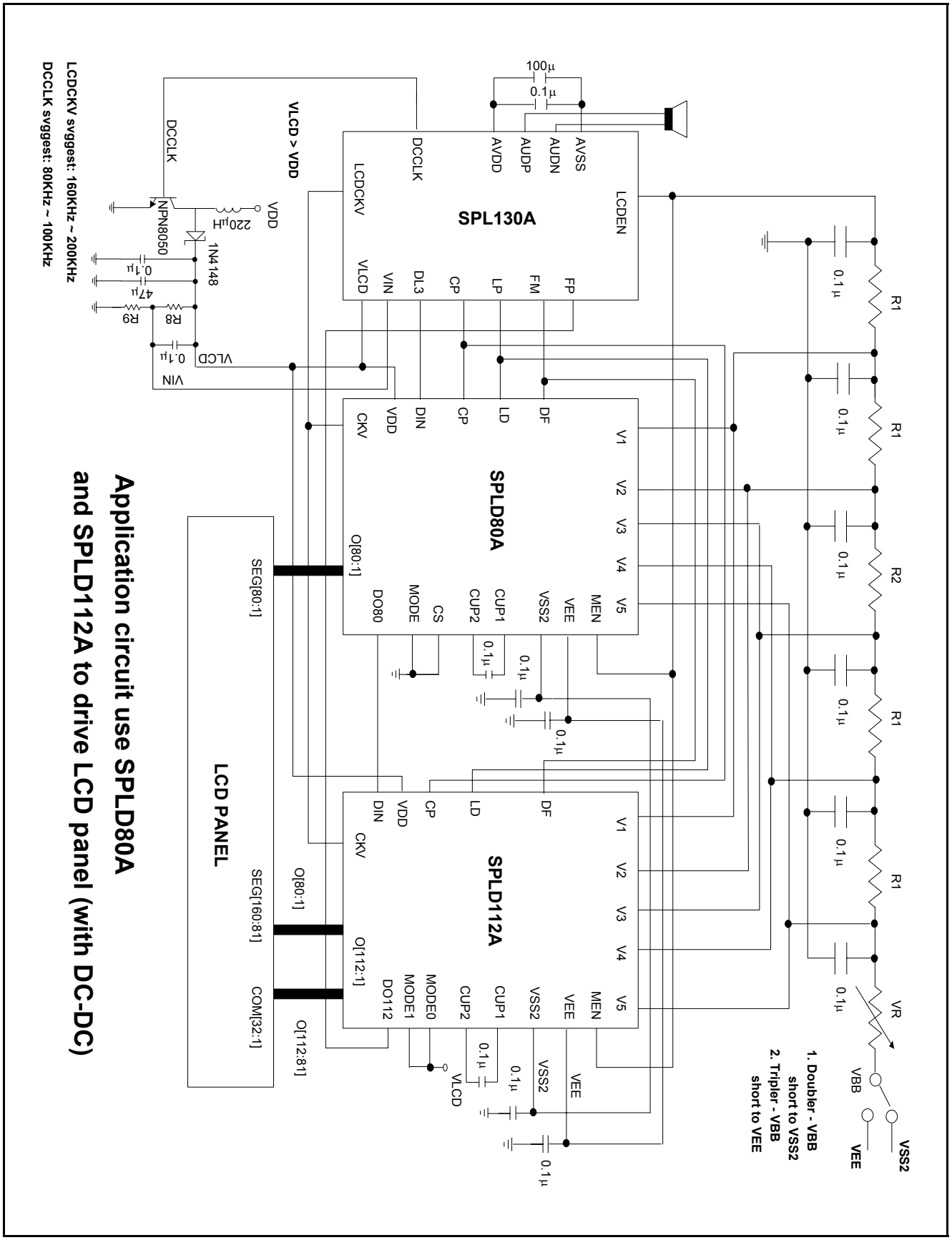


8.3. Application Circuit - (3)



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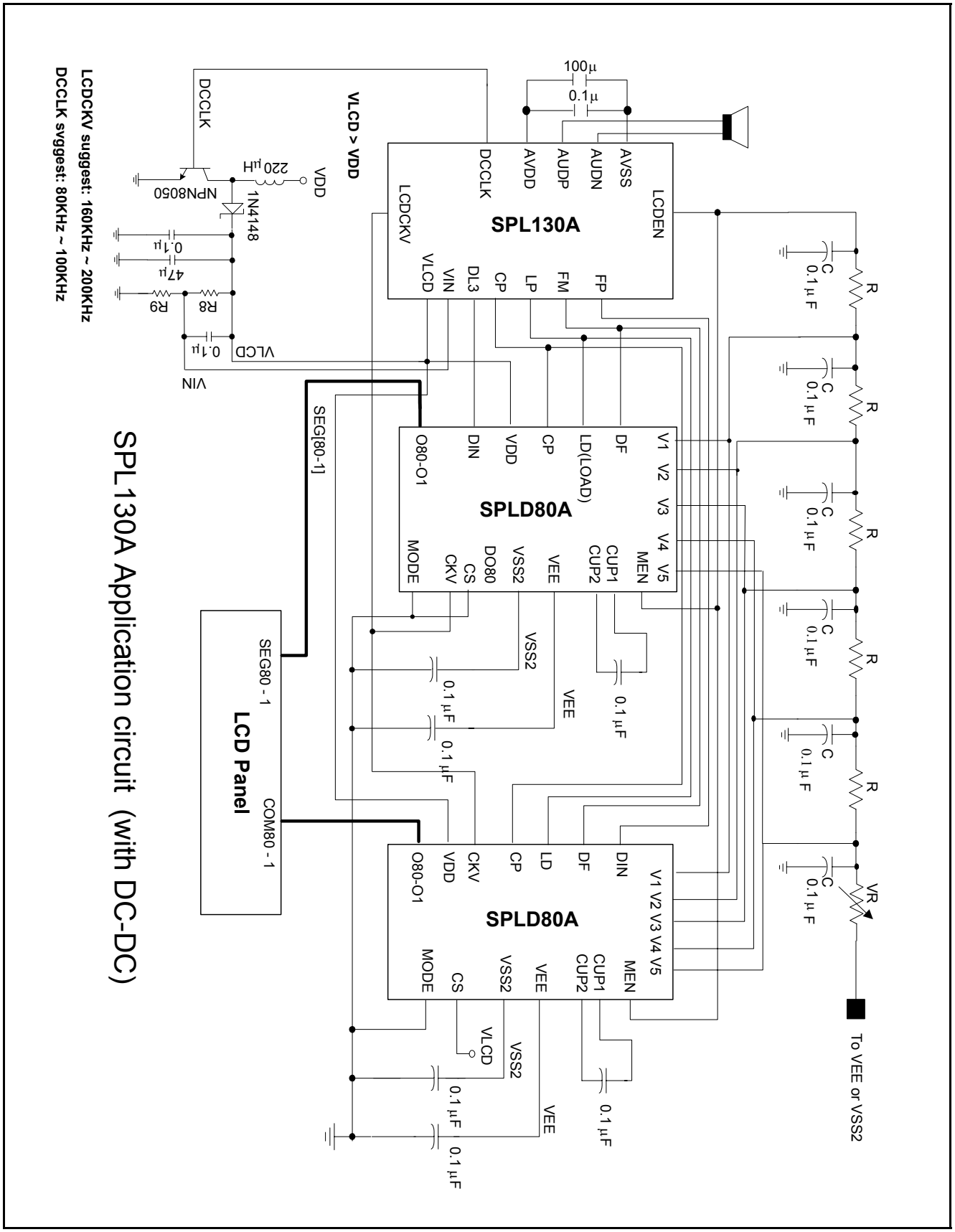

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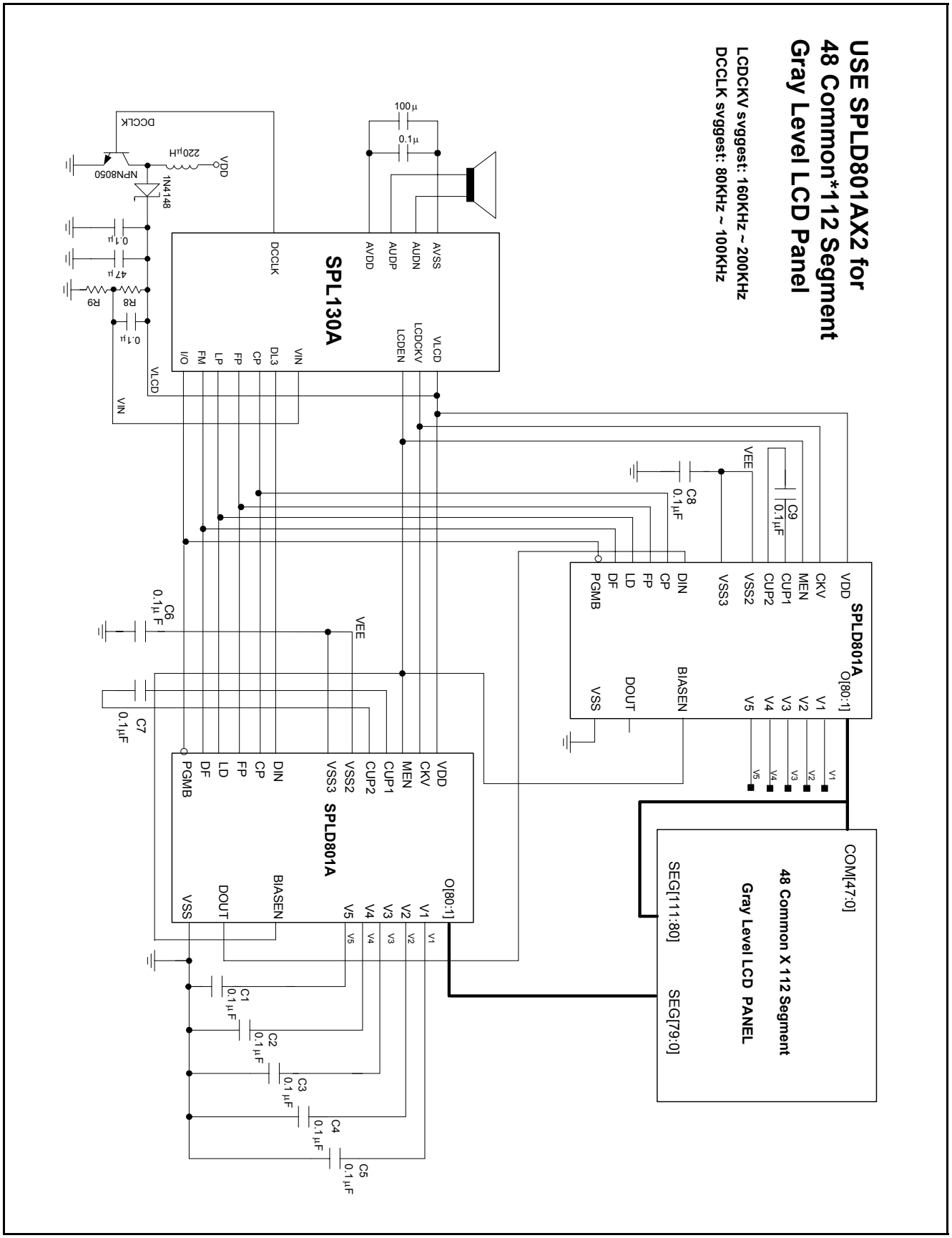

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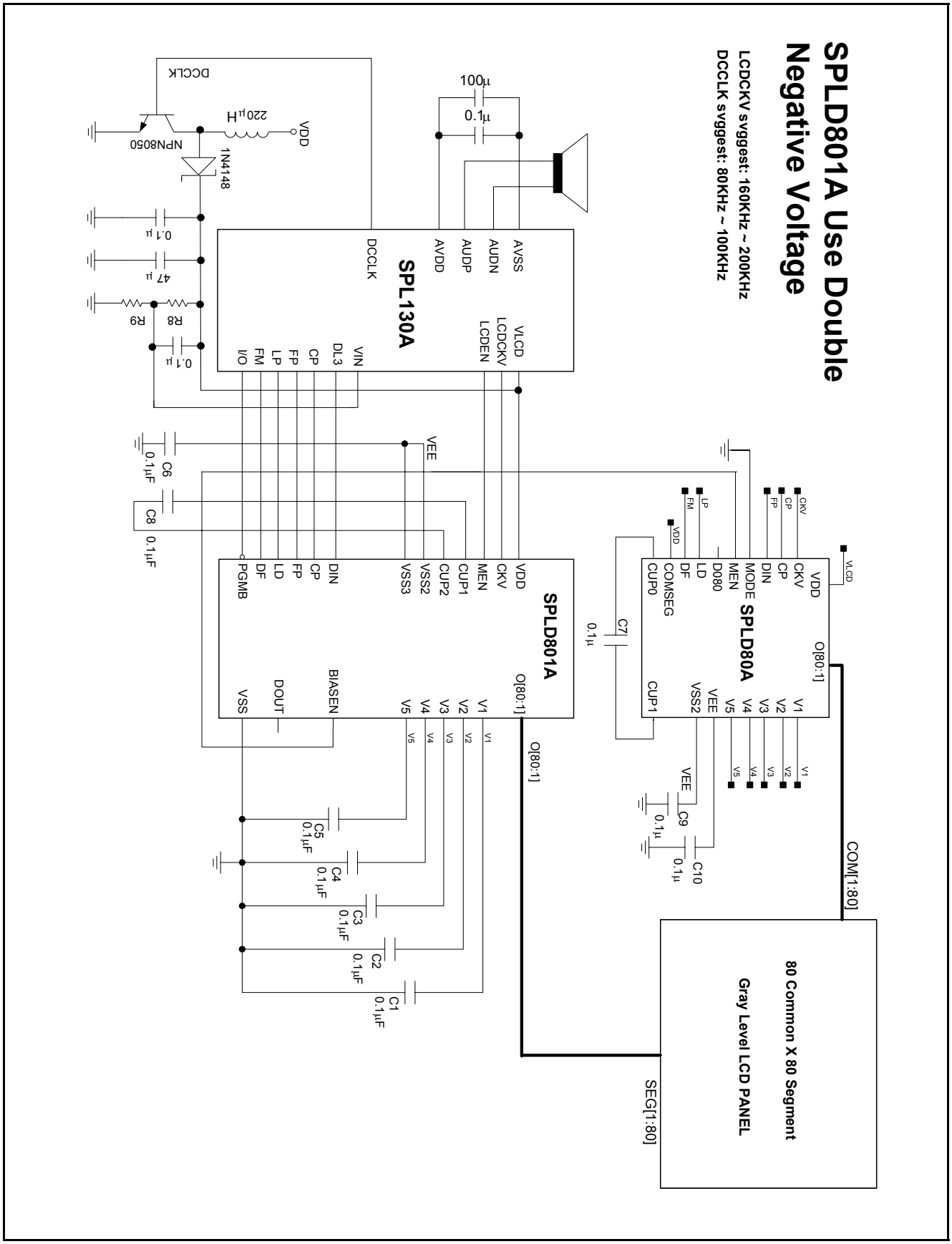

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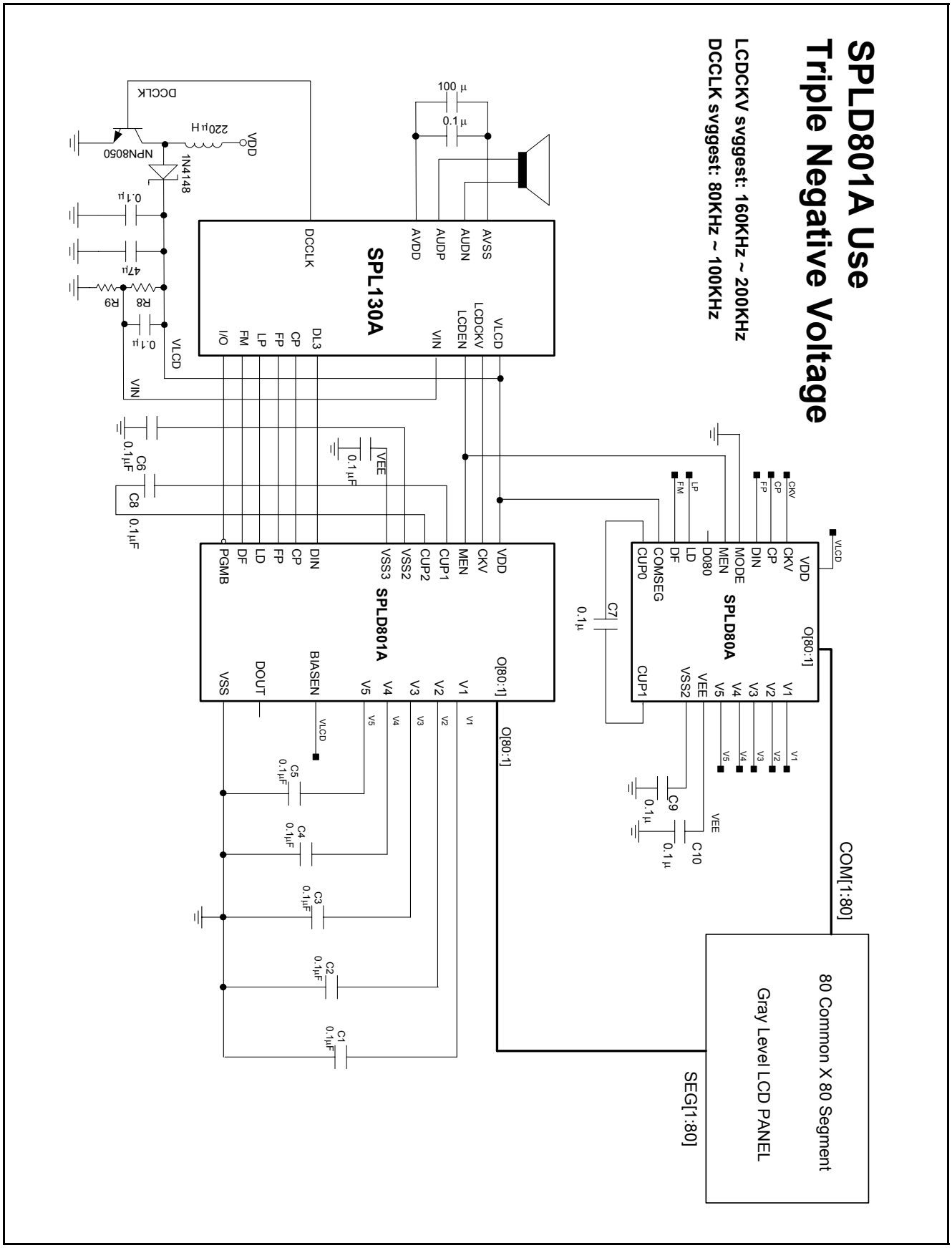
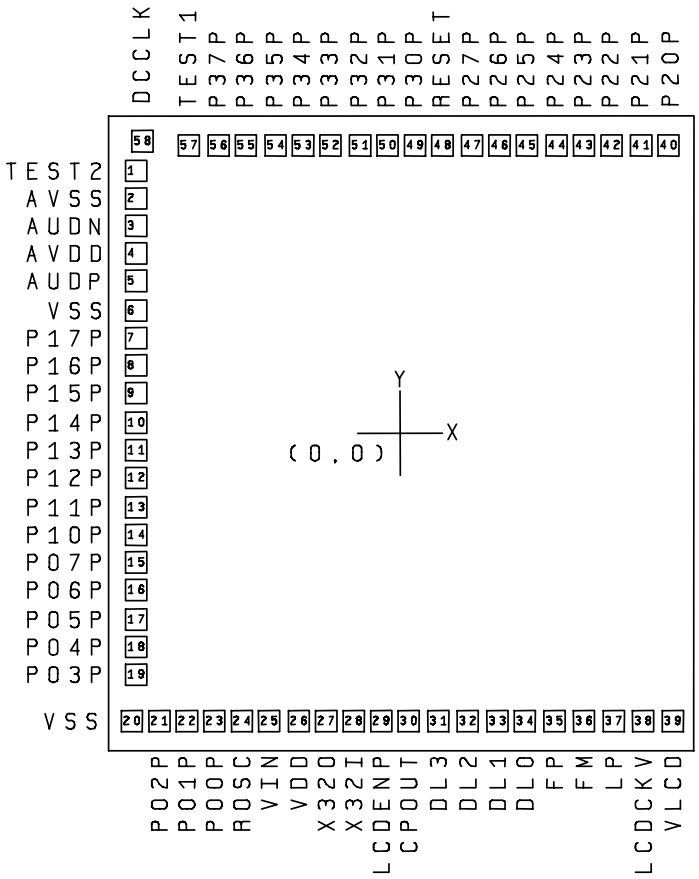


9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 2870μm X 3150μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPL130A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	TEST2	-1250	1240	30	CPOUT	37	-1364
2	AVSS	-1250	1109	31	DL3	175	-1364
3	AUDN	-1250	978	32	DL2	313	-1364
4	AVDD	-1250	847	33	DL1	451	-1364
5	AUDP	-1250	716	34	DL0	589	-1364
6	VSS	-1250	584	35	FP	727	-1364
7	P17P	-1250	453	36	FM	865	-1364
8	P16P	-1250	320	37	LP	1003	-1364
9	P15P	-1250	187	38	LCDCKV	1141	-1364
10	P14P	-1250	54	39	VLCD	1281	-1364
11	P13P	-1250	-79	40	P20P	1265	1364
12	P12P	-1250	-212	41	P21P	1132	1364
13	P11P	-1250	-345	42	P22P	999	1364
14	P10P	-1250	-478	43	P23P	866	1364
15	P07P	-1250	-611	44	P24P	733	1364
16	P06P	-1250	-744	45	P25P	600	1364
17	P05P	-1250	-877	46	P26P	467	1364
18	P04P	-1250	-1010	47	P27P	334	1364
19	P03P	-1250	-1143	48	RESET	200	1364
20	VSS	-1279	-1364	49	P30P	68	1364
21	P02P	-1148	-1364	50	P31P	-65	1364
22	P01P	-1015	-1364	51	P32P	-198	1364
23	P00P	-882	-1364	52	P33P	-331	1364
24	ROSC	-751	-1364	53	P34P	-464	1364
25	VIN	-620	-1364	54	P35P	-597	1364
26	VDD	-488	-1364	55	P36P	-730	1364
27	X32O	-357	-1364	56	P37P	-863	1364
28	X32I	-226	-1364	57	TESTP1	-1005	1364
29	LCDENP	-94	-1364	58	DCCLK	-1228	1385

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 15, 1999	0.1	Original	
MAR. 02, 1999	0.2	1. Add "*APPLICATION CIRCUITS*" 2. Add "*PAD ASSIGMENT and PAD LOCATIONS*"	5 - 8 9 - 10
MAY. 24, 1999	0.3	Add VSS Pin to "*PAD ASSIGMNENT"* and *"PAD LOCATIONS*"	9 - 10
SEP. 27, 1999	0.4	Add "*APPLICATION CIRCUITS*"	8 - 10
DEC. 05, 1999	1.0	Delete "*PRELIMINARY*"	
SEP. 22, 2000	1.1	1. VLCD Type: O (Output) -> I (Input) 2. Add "*REVISION HISTORY*" 3. Renew to a new document format	8 19
OCT. 04, 2001	1.2	1. Correct chip size 2. Add Note1 and Note3 in the "*9.1 PAD Assignment*" 3. Renew to a new document format	19 19

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