DATA SHEET

凌陽科技
SUNPLUS

SPL133A

256KB LCD Controller

Preliminary

MAY. 14, 2001

Version 0.1

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256KB LCD CONTROLLER

1. GENERAL DESCRIPTION

The SPL133A, an 8-bit microprocessor with advanced CMOS technology, offers a wild assortment of features, including a large size of RAM and ROM, I/Os, PWM audio output, UART, low voltage detector and plus many others. The amount of 256K-byte of ROM and 4K-byte of RAM offer lots of room to store plenty of data and program. Up to 6.0MHz running speed ensures the sophisticated functions and graphics are performed in a flawless way. The 32 programmable I/Os arise the abilities in driving and communicating with other components. The built-in UART facilitates the data communication between devices. In addition, the low voltage detector reports a battery status that gives a clear signal of when to change the battery. The SPL133A includes two sets of 16-bit TIMER/COUNTER circuit that can be programmed as two independent timers, or a 32-bit timer. Furthermore, LCD interface structure can be programmed to implement varieties of dot matrix panel applications from 48*32 to 160*80 with single or more LCD drivers. Other impressed features such as external interrupt sources, sleep mode, key wakeup capability, and E.L driver make SPL133A ranked the best cost and performance ratio in the LCD-controller industry. With fully loads of SUNPLUS state-of-the-art technology and commitment, users are guaranteed to receive completed and satisfactory support.

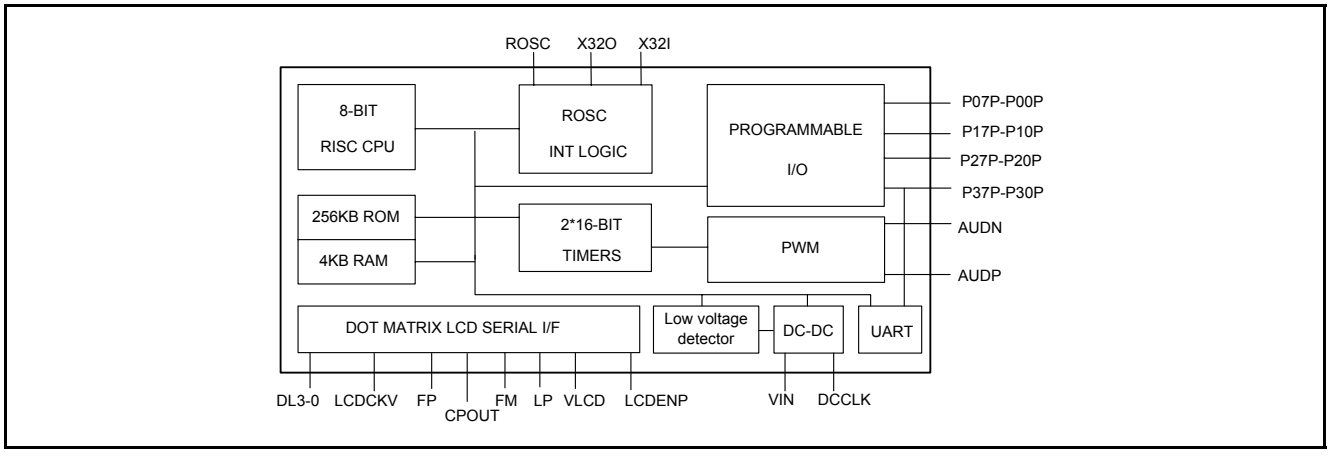
2. APPLICATION FIELD

- Data Bank
- LCD toy/game
- Educational computer
- Consumer, Industry LCD controller

3. FEATURES

- 8-bit RISC controller
- Operating Voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Working frequency: 4.0MHz @ 2.4V, 6.0MHz @ 3.6V
- SRAM size: 4.0K bytes
- ROM size: 256.0K bytes
- 32 general I/O pins
- Built-in RC Oscillator
- Two-channel speech/tone generator
- 8-bit PWM output
- UART receiver and transmitter
- Low Voltage Detector (2.4V, 2.6V)
  Low Voltage Reset (2.3V)
- Bus Extender interface for external memory
- 8 interrupt sources
- Two 16-bit Timer/Counters (can be one 32-bit)
- Internal time base generator
- Built-in LCD controller, serially interface with external LCD driver, to drive large dot matrix LCD panel
- Built-in 32768Hz crystal Oscillator
- Very low standby current < 1.0μA at power down model
  (Stop RC oscillator; stop 32768Hz crystal oscillator)
- Wake-up source:
  - Key change wakeup
  - Timer0 wake up
  - Timer base wake up

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

P: Port

Mnemonic	PIN No.	Type	Description
P17P - P00P	16 - 1	I/O	**General I/O** Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both.
P27P - P20P	29 - 36	I/O	General I/O /Address/Data Mux IO Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both.
P37P - P30P	20 - 27	I/O	**General I/O** Input Mode: Pure, Pull-high, Pull-low Output Mode: Pure, ODP (Open drain PMOS), ODN (Open drain NMOS) **Note:** ODP or ODN can be existed only one state, not both. **Additional Function** P30P/ EXTI: External interrupt pin P31P/ MC0: Memory interface control signal pin P32P/ECLK: External clock input pin for Timer0 P33P/E.Ldrv0/TO0out: E. L. driver0. When Timer0 overflows, output signals to this pin P34P/E.Ldrv1/TO1out: E. L. driver1. When Timer1 overflows, output signals to this pin. P35P/TX (UART Transmitter): Baud rate ranged from 1200bps to 115.2Kbps. P36P/MC1 (Memory control): Memory interface control signal pin. P37P/RX (UART Receiver)
ROSC	42	I	R-osc input, connect to VDD through a resistor.
$\overline{\text{RESET}}$	38	I	System reset input pin. Internal pull high. Low active. (see RESET)
AUDP	48	O	PWM Audio output
AUDN	46	O	PWM Audio output
X32I	41	I	32.768KHz crystal input (20p capacitor required)
X32O	40	O	32.768KHz crystal output (20p capacitor required)
TEST1 TEST2	37 17	I I	Test input. Normally floating
AVDD	39	I	Power input for analog
VDDP	47	I	Power input for PWM
VDD1	19	I	Digital power input
VDD2	28	I	Digital power input
AVSS	44	I	Ground input for analog
VSSP	45	I	Ground input for PWM
VSS1	49	I	Digital Ground input
DL3 - 0	55 - 58	O	1-bit LCD data output (DL3), or 4-bit LCD data output (DL3 - 0). *See **LCD Interface Section.***
LCDENP	59	O	LCD enable signal. *See **LCD Interface Section***
CPOUT	54	O	LCD data shift clock. See ***LCD Interface Section***
FM	50	O	LCD alternate signal. See ***LCD Interface Section***
LP	52	O	LCD data load. See ***LCD Interface Section***
FP	51	O	LCD FRAME pulse. See ***LCD Interface Section***

Mnemonic	PIN No.	Type	Description
VIN	43	I	DC-DC input to compare with reference voltage. See ***DC_DC LCD Driver Section***
DCCLK	18	O	DC-DC charge pump clock. See ***DC_DC LCD Driver Section***
LCDCKV	53	O	Charge pump clock for SPLD80, SPLD112. See ***LCD Interface Section***
VLCD	60	I	DC-DC output voltage to supply power for LCD driver (SPLD80 or SPLD112). See ***DC_DC LCD Driver Section***

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPL133A is an 8-bit CPU, capable of running at highest speed of 6.0MHz. The instruction set is 6502 compatible which involves A, X and Y registers.

6.2. Memory

The SPL133A contains 256KB ROM and 4KB RAM. Cooperating with Sunplus bus extender, SPBA01A, the external memory, either RAM or ROM, can be extended up to 4MB.

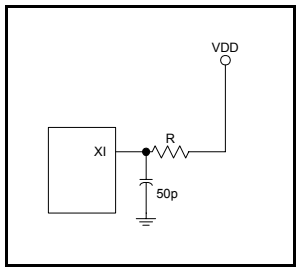
1). RAM: 4K bytes
2). ROM: 256K bytes, 32KB/bank
3). EXTERNAL MEMORY: Using Port2.0 - Port2.7, Port3.1 and Port3.6, (total of 10 pins) to extend ROM or RAM capacity.

6.3. Clock, Power Mode, LVD/Power Down

6.3.1. Clock

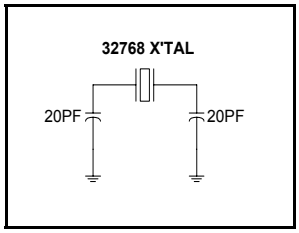
6.3.1.1. System clock

One clock source available: R oscillator. The unique design of R oscillator provides higher frequency and has less effect to the power deviation than other ordinary R-oscillators. The system clock can be used as the sources of timers and UART.



6.3.1.2. 32768 RTC

Two types of RTC available: X'TAL and ROSC (from System Clock source). The 32768Hz X'TAL provides more precious timing than ROSC does. The X'TAL type is highly recommended. The 32768Hz RTC is the source of time-base, TBL and TBH. The time-base can be used for interrupt, wake-up source, timer/counter clock and watchdog timer.



TBL: 2Hz, 4Hz, 8Hz, 16Hz
TBH: 128Hz, 256Hz, 512Hz, 1KHz

6.3.2. Power mode

Three power modes available: Operating, Halt and Standby. A summary depicts the major differences between three modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz OSC.	ON	ON	OFF
LCD Driver	ON	OFF	OFF

6.3.2.1. Operating mode

In operating state, all functions including CPU, R-oscillator, timer/counter, and LCD controllers are activated.

6.3.2.2. Halt mode

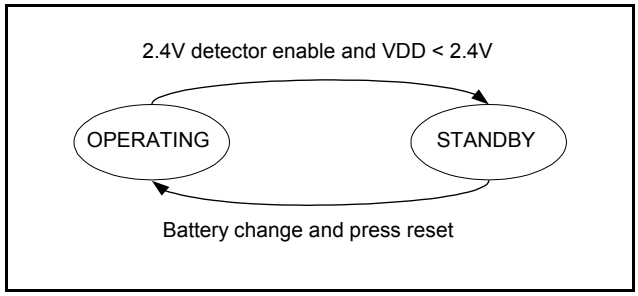
Users have to enable TBL first and then set CPU clock control CKS2 - CKS0 (in Register $04) to "111" to enter halt state. During halt mode, the 32768Hz oscillator must be enabled to generate time-base wakeup. In addition, users can also enable the key wakeup source for extra wakeup source.

6.3.2.3. Standby mode

To enter standby mode, set CKS2 - CKS0 = "111". The key wake-up is the only wake-up source for returning to the operating mode which means users have to enable key wakeup (b0 in Register $18) before entering standby. In standing-by, all functions are shut down, and RAM and I/O remain in their previous states. The current consumption is minimized in standby mode. If any wakeup event occurs during the halt or standby mode, the first instruction to be executed will be the one after halt or standby instruction.

6.3.3. Low voltage detect/Power down

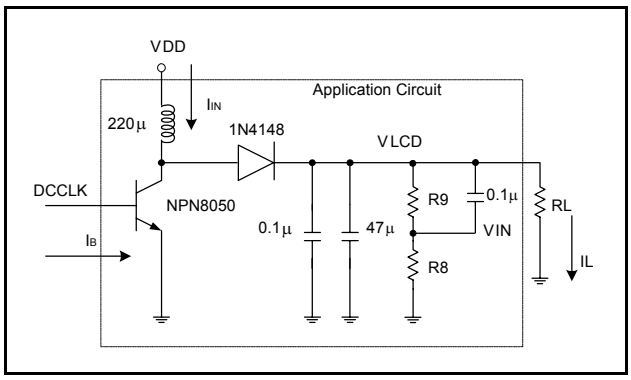
The SPL133A provides a 2.6V/2.4V voltage detector to detect a low voltage event. Users can turn on 2.6V detection and read bit6 of Register $18 periodically or enable NMI to monitor if VDD is lower than 2.6V. In addition, if 2.4V detection is turned on and VDD drop below 2.4V, system will shut down all activities automatically and enters standby to reduce current consumption. User can use this feature to implement low battery check/battery change function.



State Diagram of Low Voltage Power Down

6.4. DC_DC LCD Driver

Generally, the DC_DC is applied to LCD drivers such as SPLD80, or SPLD112 for charge pump source. The DC-DC circuit in SPL133A generates a supply voltage that is stable and independent to the battery voltage for LCD driver. Its application circuit is shown in following figure. Users can also use a regulator instead and connect the VLCD pin to the output of regulator. The DCCLK generates charge pump clock of DC_DC. A recommended frequency range is from 80KHz through 100KHz. If the frequency is given too slow, the supply voltage will have large ripple. On the other hand, if the frequency is too fast, the charge pump circuit will reduce its efficiency. The DCCLK frequency can be determined by programming Register $32. The ratio of the resistors, R9 and R8, influences the DC-DC pump voltage. If the ratio is large, the pump voltage will also be larger. It's also suggested having the value of VLCD larger than VDD; therefore, VLCD will have less effective to VDD variation.



6.5. Interrupt

6.5.1. Interrupt type

Two types of interrupt available: IRQ and NMI

6.5.2. IRQ

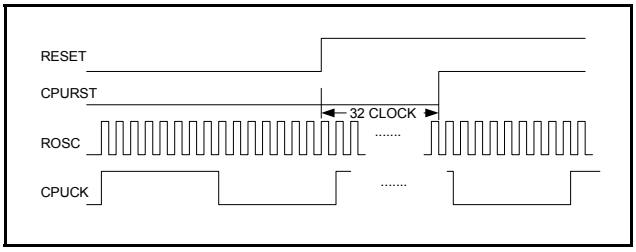
Sources are UART receiver and transmitter, Timer0, Timer1, Time-base TBL and TBH, frame pulse interrupt, and external interrupt.

6.5.3. NMI

When working voltage drops below 2.6V, NMI generated and interrupts the CPU.

6.5.4. RESET

When reset pin receives a low signal, the control registers are initialized, but the data stored in SRAM will not be changed. Because there is a pull-high resistor connected to reset pin, a 0.1µF capacitor is required to connect with GND.



6.5.5. Interrupt vector

User Program:

FFFA	NMI
FFFC	RESET
FFFE	IRQ

Test Program:

FFF2	NMI
FFF4	RESET
FFF6	IRQ

6.6. I/O

There are four 8-bit programmable I/O ports (PORT3 - 0) in SPL133A. Each of them can be programmed individually to pure output buffer, ODP (open drain PMOS), ODN (open drain NMOS), pure input buffer, input with pull-low and input with pull-high. The IOs also have alternative functions. PORT1 can be used as wakeup key. The bit1 and bit6 of PORT3 and PORT2 can be connected to SPBA01 to extend RAM or ROM. The bit5 and bit7 of PORT3 can be used as UART's transmit output and receive input; bit0 can be external interrupt whereas bit2 can be connected to external clock to be the clock source of Timer0.

6.6.1. I/O configuration

6.6.1.1. State after reset

Port0, Port1, Port2 and Port3 are all input mode with pull low state after RESET.

6.6.1.2. I/O port operation

Input Mode:

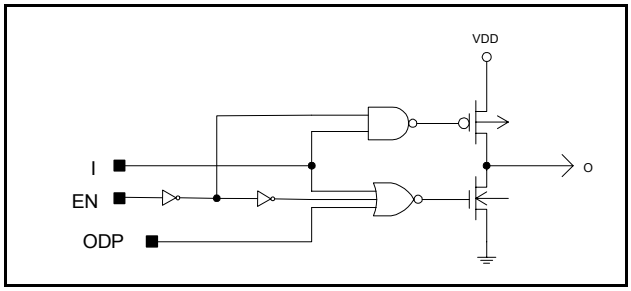
- Pure
- Pull-high
- Pull-low

Output Mode:

- Pure
- ODP (Open drain PMOS)
- ODN (Open drain NMOS)

I/O Structure of the state

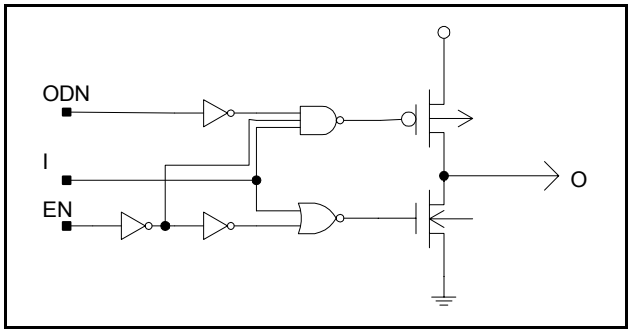
1). Output Mode with ODP State



When ODP = H, Output is Open Drain PMOS state

When ODP = L, Output is Pure Output state

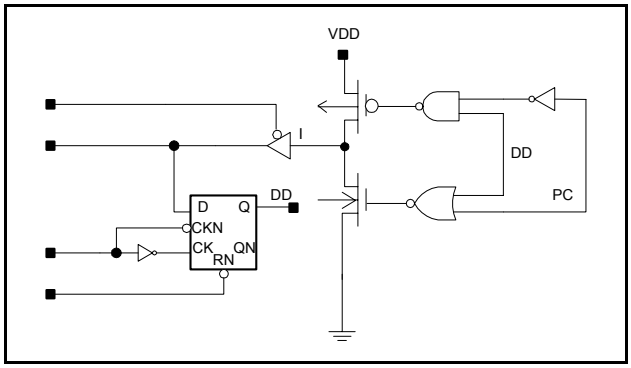
2). Output mode with ODN state



When ODN = H, Output is Open Drain NMOS.

When ODN = L, Output is Pure Output.

3). Input Mode with pure, pull high/low states



When PC = H, input is pure state.

When PC = L, input is pull high if DD = H

When PC = L, input is pull low if DD = L

6.7. LCD Interface

6.7.1. LCD controller feature

The built-in LCD controller supports 1-bit or 4-bit data for LCD driver. The LCD data shift clock and frame rate can be programmed according to the amount of data to be displayed on LCD panel and can save more power. The RAM size in SPL133A is 4K bytes. User can determine the size of LCD RAM by giving a start-address and end-address to the configuration port. After the LCD RAM is determined, users have to specify the number of segments in PORT$0E. When the above configurations are completed, the number of commons is determined automatically by hardware. Note that the LCD controller cannot support signals for LCD display while in halt or standby mode.

6.7.2. LCD controller signals

SPL133A provides the following signals for 1-bit LCD driver (e.g. SPLD80, SPLD802, SPLD112) or 4-bit LCD driver (e.g. SPLC206): FM, LP, CPOUT, DL3 - 0, FP, LCDENP, and LCDCKV.

6.7.2.1. FM

The LCD alternate crystal direction output signal is toggled to alternate the crystal polarization on the panel.

6.7.2.2. LP

The LCD line pulse signal is used to latch a line of shifted data onto an LCD panel.

6.7.2.3. CPOUT

The LCD shift clock signal is the clock output to which the output data to the LCD panel is synchronized.

6.7.2.4. DL3 - 0

The LCD data bus lines transfer pixel data to the LCD panel so that it can be displayed. DL3 is for 1-bit data transferring. DL3 - 0 are for 4-bit data transferring.

6.7.2.5. FP

The LCD frame pulse signal indicates the start of a new display frame.

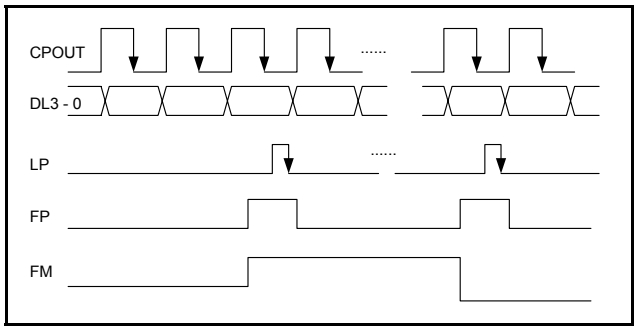
6.7.2.6. LCDENP

LCD **enable** signal

6.7.2.7. LCDCKV

Charge pump clock for LCD driver, e.g. SPLD80, SPLD112.

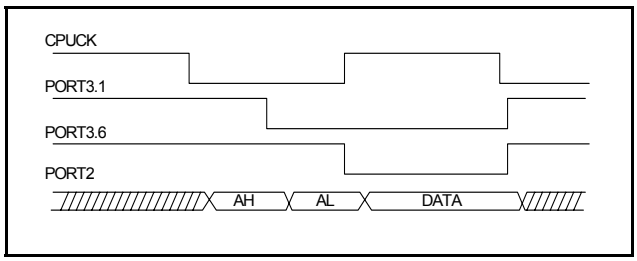
6.7.3. LCD controller signal timing diagram



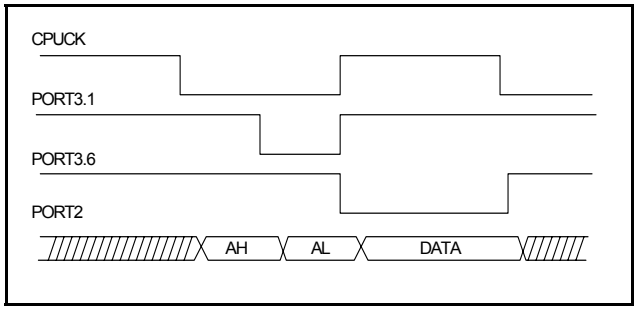
6.8. Bus Interface

The bus interface is a bridge between SPL133A and SPLB01A. The interface is accomplished by Port2, Port3.1, and Port3.6. The Port3.1 and Port3.6 are the control signals for Port2 which can be three states while communicating with SPLB01A: Address High-Byte (AH), Address-Low-Byte (AL) and 8-bit data. The following diagrams describe the timing relations between control signals, AH, AL and data.

6.8.1. Write mode



6.8.2. Read mode



6.9. UART

SPL133A includes 1-channel UART for serial communications. The bit rate ranges as low as from 1200bps and up to 115.2kbps. UART operations are controlled by UART Command Port, $19, and $1A. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be set in Command Port. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt generated when a byte is received or transmitted. By reading the Status Port, $1A, users know whether the interrupt is generated by Rx or Tx. Framing, overrun and parity errors are detected as each byte is received. All error statuses can be read from Status Port, $1A.

The UART supports auto clock calibration. If the auto clock calibration is selected, the standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to Baud Rate Control Ports, $1E and $1F. The supported standard baud rates and their minimum R-oscillator clock frequency are shown in the following table.

Baud Rate (bps)	Min. Frosc (Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration clocking scheme is not selected, users can get desired baud rates by writing appropriate values to Pre-scalar Registers, $1C and $1D. Non-standard baud rates can be obtained this way. When using non-calibration mode, users should aware that the frequency of R-oscillator may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.10. TIMER

SPL133A provides two 16-bit times, TM0 and TM1, which can be programmed as two independent timers or to a single 32-bit timer. TM0 can be used as either timer or counter whereas TM1 can only be a timer. The timer's time base is selected from 2Hz up to R-oscillator's clock. For more information, refer to the SPL133A Programming Guide.

6.11. PWM

6.11.1. PWM output

SPL133A contains one pair of PWM outputs supporting with two sound channels. Each channel can play speech or tone individually. SPL133A uses Pulse Width Modulation that could directly drive speaker or buzzer without any buffer or amplification circuit.

6.11.2. Speech and melody

For speech synthesis, SPL133A provides several timer interrupts to make sample frequency more precisely. Users can record or synthesize the sound and digitize it into ROM. After that, the sound can be played back. Two algorithms are recommended for high fidelity and good compression of sound: PCM and ADPCM. PCM provides higher quality of speech but less speech length. ADPCM, on the other hand, offers less quality but longer speech length.

For melody synthesis, SPL133A provides dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically

6.12. Mask Option Summary

6.12.1. WatchDog

The watchdog timer is especially designed for recovering the system from abnormal operation. The watchdog generates a reset signal every one second. Therefore, it must be cleared within one second, 0.5 second is recommended normally. The watchdog works only when the 32768Hz OSC is enabled and read PORT$02 to clear watchdog.

6.12.2. 32768 X'TAL

SPL133A contains 32768Hz X'TAL oscillator for generating real-time clock and it can be disable by code-option.

6.12.3. Low voltage reset

There is built-in 2.3V low-voltage reset in SPL133A to avoid abnormal operation. The function could also be disable by code-option if unwanted.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

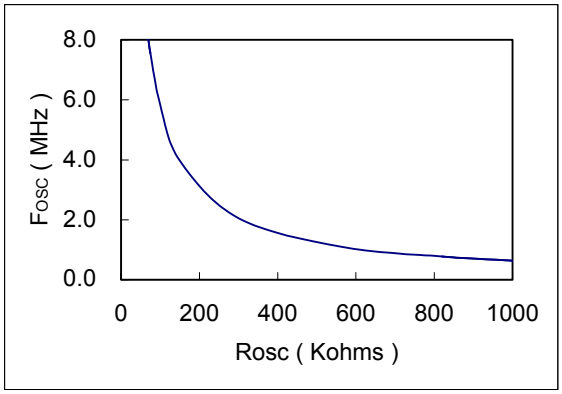
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1200.0	-	μA	$F_{CPU} = F_{OSC}/2$ = 2.0MHz @ 3.0V No load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.6V, all osc off, 32768Hz off
Output High I (I/O Port 2)	I_{OH}	-	-5.0	-	mA	VDD = 3.0V V_{OH} = 2.4V
Output Sink I (I/O Port 2)	I_{OL}	-	7.5	-	mA	VDD = 3.0V V_{OL} = 0.8V
Output High I (I/O Port 0, 1, 3)	I_{OH}	-	-1.5	-	mA	VDD = 3.0V V_{OH} = 2.4V
Output Sink I (I/O Port 0, 1, 3)	I_{OL}	-	2.0	-	mA	VDD = 3.0V V_{OL} = 0.8V
PWM Drive Current	I_{POH}	-	-40.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
PWM Sink Current	I_{POL}	-	40.0	-	mA	VDD = 3.0V, V_{OL} = 0.8V

7.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

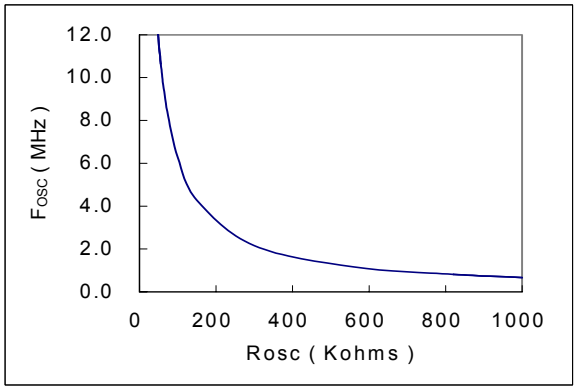
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	2500.0	-	μA	$F_{CPU} = F_{OSC}/2$ = 2.0MHz @ 4.5V No load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 5.5V, all osc off, 32768Hz off
Output High I (I/O Port 2)	I_{OH}	-	- 10.0	-	mA	VDD = 4.5V V_{OH} = 3.6V
Output Sink I (I/O Port 2)	I_{OL}	-	15.0	-	mA	VDD = 4.5V V_{OL} = 0.9V
Output High I (I/O Port 0, 1, 3)	I_{OH}	-	-2.0	-	mA	VDD = 4.5V V_{OH} = 3.6V
Output Sink I (I/O Port 0, 1, 3)	I_{OL}	-	2.5	-	mA	VDD = 4.5V V_{OL} = 0.9V
PWM Drive Current	I_{POH}	-	-70.0	-	mA	VDD = 4.5V, V_{OH} = 3.6V
PWM Sink Current	I_{POL}	-	70.0	-	mA	VDD = 4.5V, V_{OL} = 0.9V

7.4. The Relationships between the R_{OSC} and the F_{OSC}

7.4.1. VDD = 3.0V, T_A = 25℃

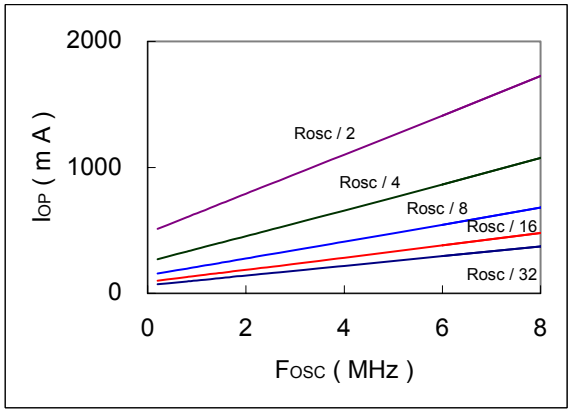


7.4.2. VDD = 4.5V, T_A = 25℃

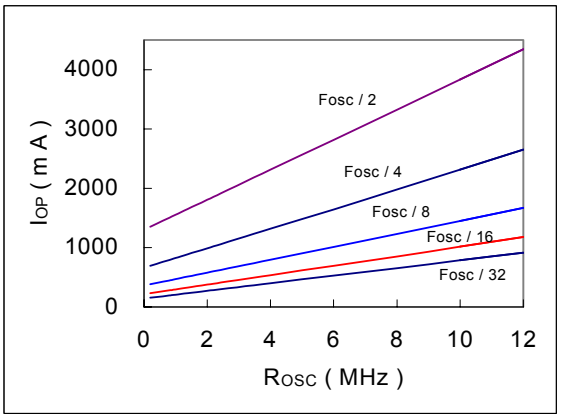


7.5. The Relationships between the F_{OSC} and the I_{OP}

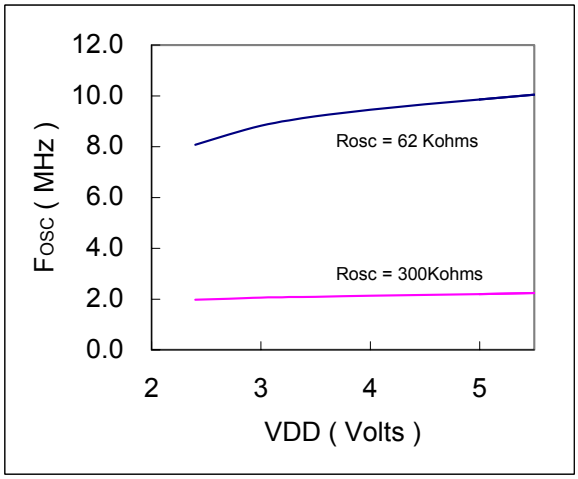
7.5.1. VDD = 3.0V



7.5.2. VDD = 4.5V

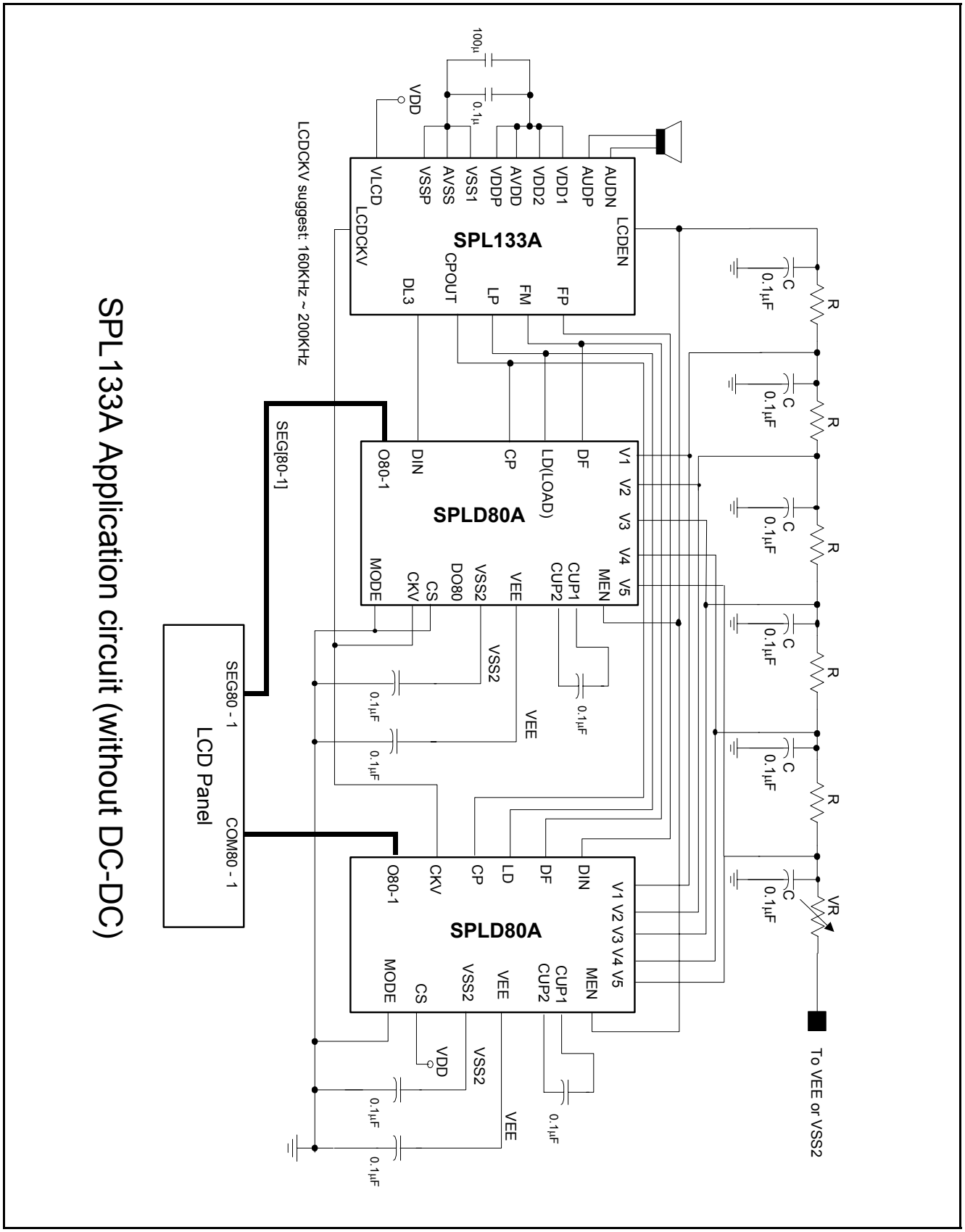


7.6. The Relationships between the F_{OSC} and the VDD

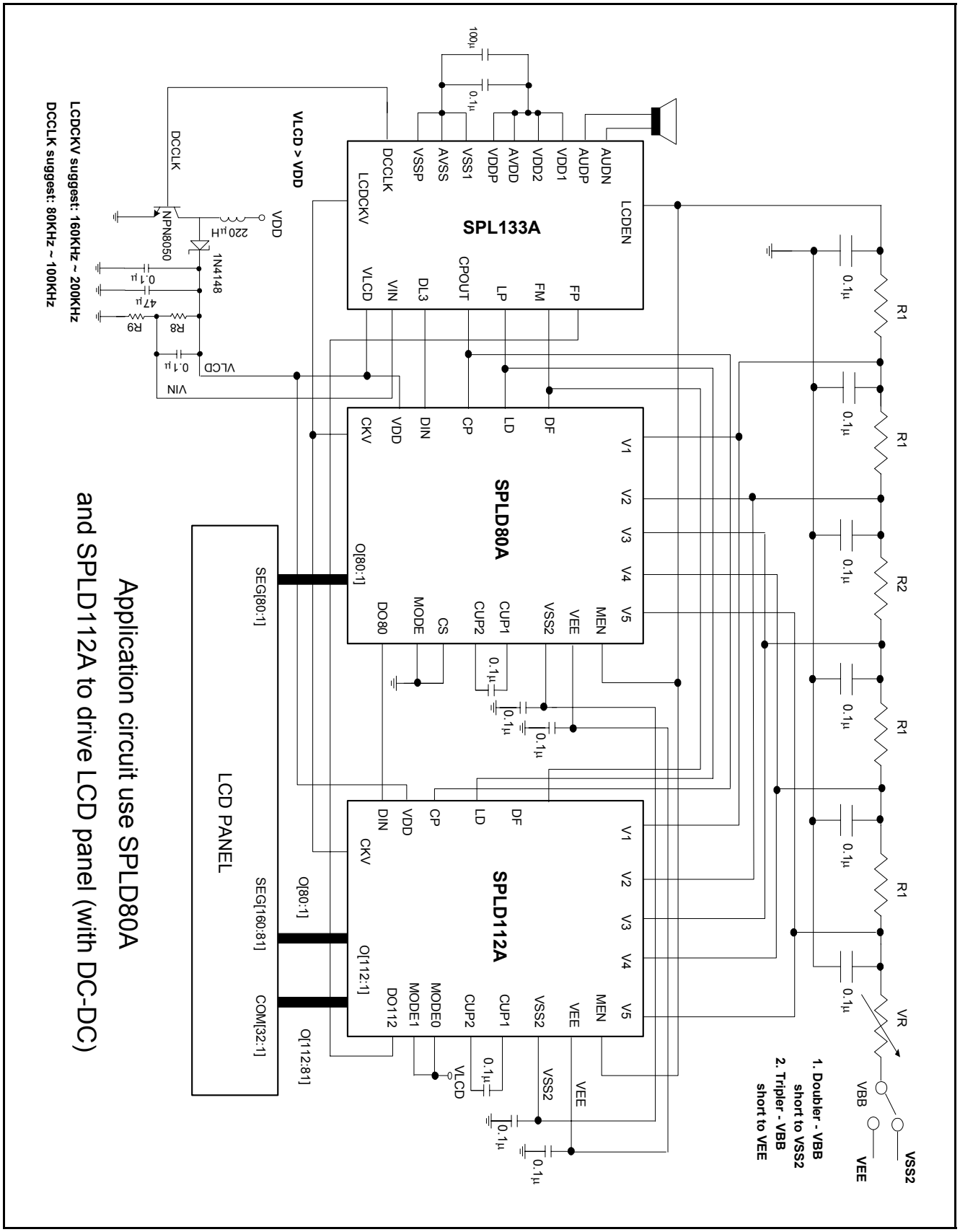


8. APPLICATION CIRCUITS

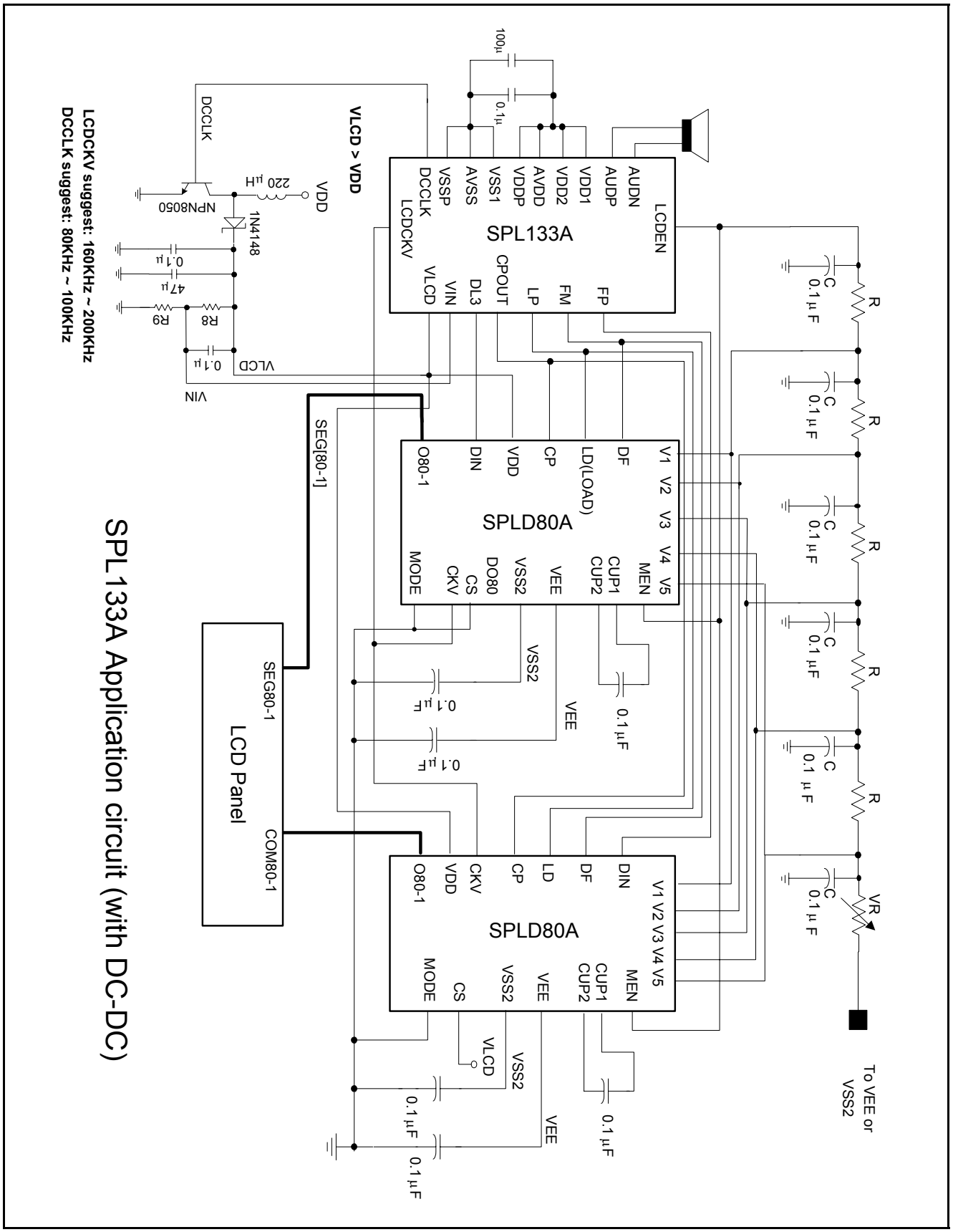
8.1. Application Circuit - (1)



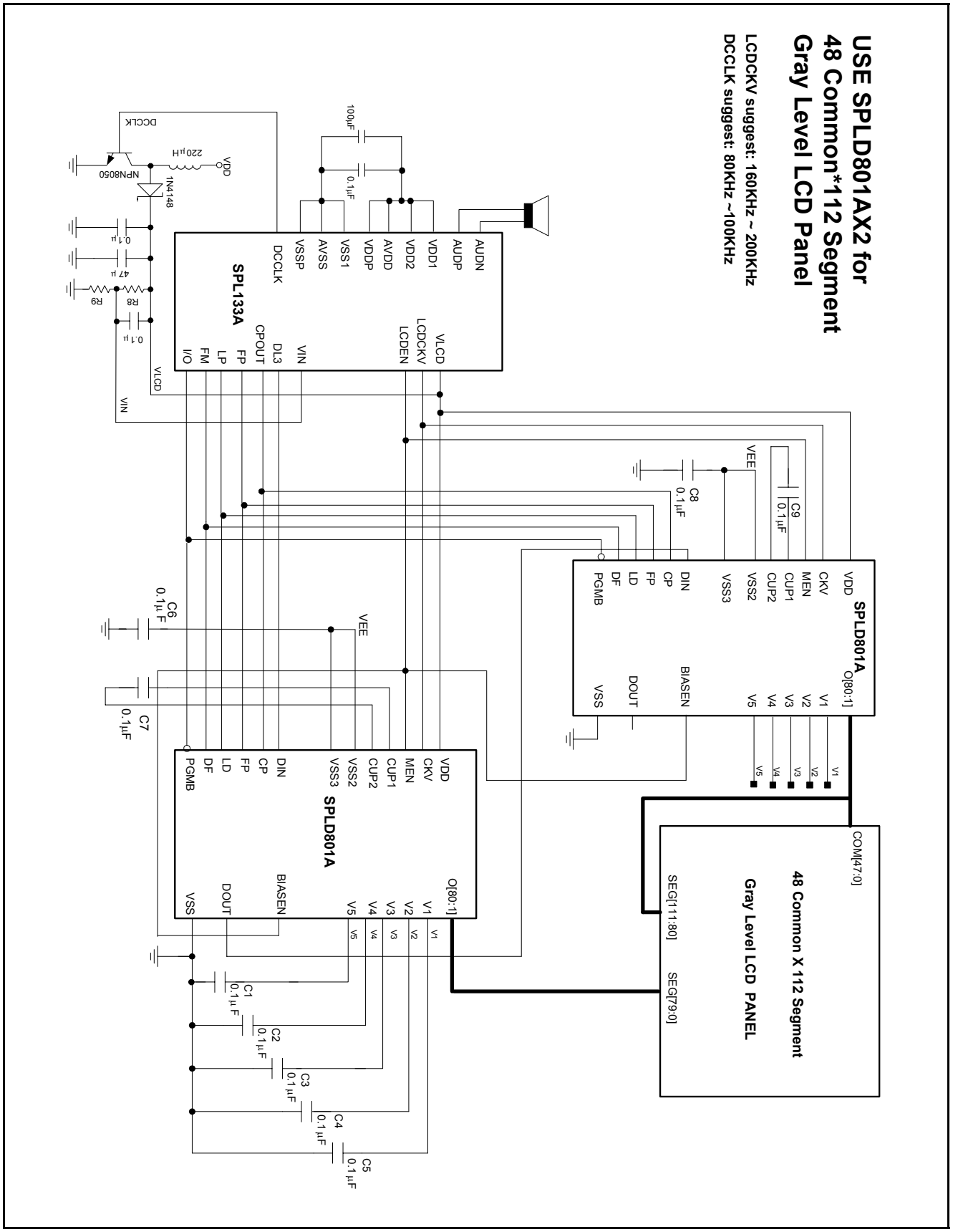
8.2. Application Circuit - (2)



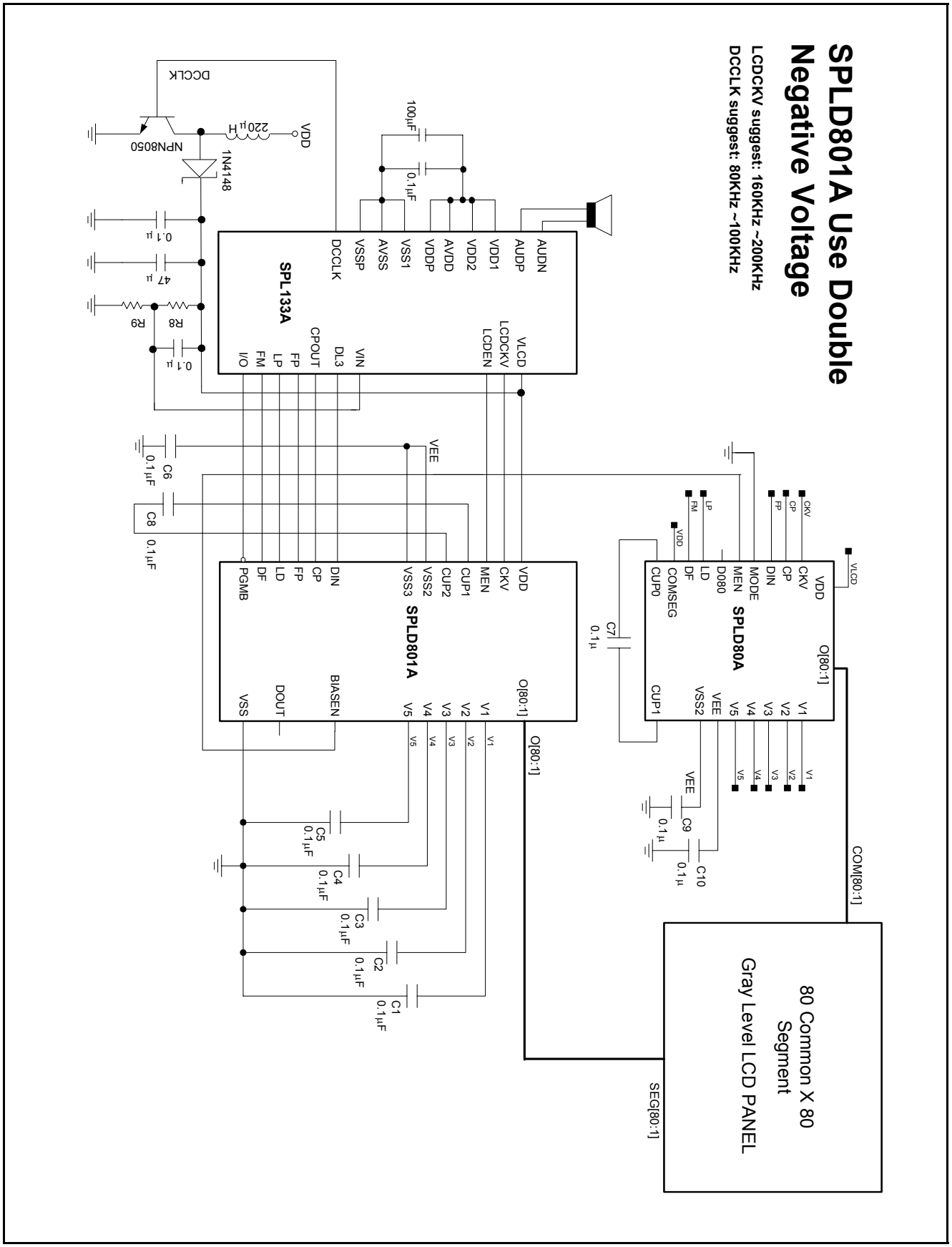
8.3. Application Circuit - (3)



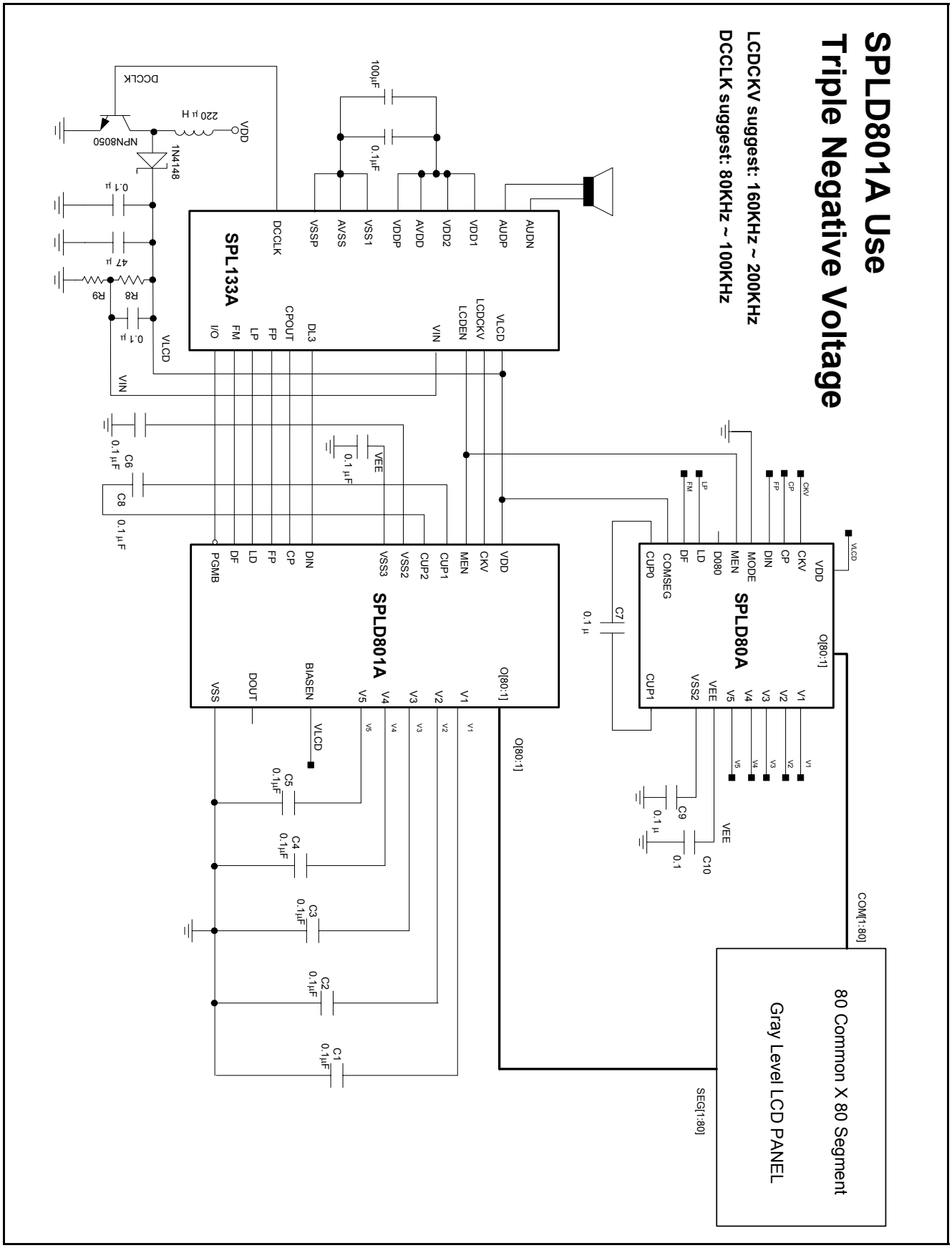
8.4. Application Circuit - (4)



8.5. Application Circuit - (5)

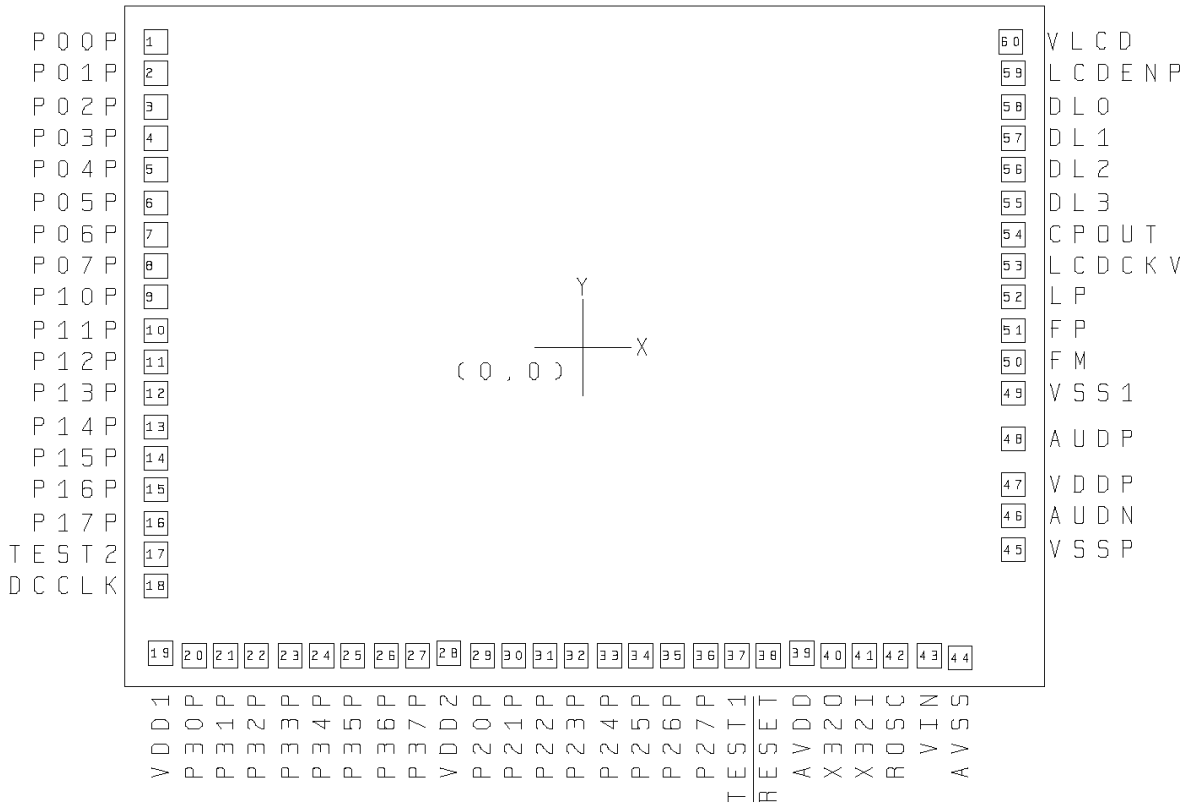


8.6. Application Circuit - (6)



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 3930μm x 2930μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPL133A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	P00P	-1782	1265	31	P22P	-163	-1282
2	P01P	-1782	1132	32	P23P	-30	-1282
3	P02P	-1782	999	33	P24P	103	-1282
4	P03P	-1782	866	34	P25P	236	-1282
5	P04P	-1782	733	35	P26P	369	-1282
6	P05P	-1782	600	36	P27P	502	-1282
7	P06P	-1782	467	37	TEST1	635	-1282
8	P07P	-1782	334	38	$\overline{\text{RESET}}$	770	-1282
9	P10P	-1782	201	39	AVDD	901	-1274
10	P11P	-1782	68	40	X32O	1034	-1282
11	P12P	-1782	-65	41	X32I	1167	-1282
12	P13P	-1782	-198	42	ROSC	1300	-1282
13	P14P	-1782	-331	43	VIN	1433	-1282
14	P15P	-1782	-464	44	AVSS	1566	-1292
15	P16P	-1782	-597	45	VSSP	1783	-843
16	P17P	-1782	-730	46	AUDN	1783	-708
17	TEST2	-1782	-863	47	VDDP	1783	-573
18	DCCLK	-1782	-996	48	AUDP	1783	-382
19	VDD1	-1761	-1274	49	VSS1	1781	-198
20	P30P	-1626	-1282	50	FM	1781	-65
21	P31P	-1493	-1282	51	FP	1781	68
22	P32P	-1360	-1282	52	LP	1781	201
23	P33P	-1227	-1282	53	LCDCKV	1781	334
24	P34P	-1094	-1282	54	CPOUT	1781	467
25	P35P	-961	-1282	55	DL3	1781	600
26	P36P	-828	-1282	56	DL2	1781	733
27	P37P	-695	-1282	57	DL1	1781	866
28	VDD2	-562	-1274	58	DL0	1781	999
29	P20P	-429	-1282	59	LCDENP	1781	1132
30	P21P	-296	-1282	60	VLCD	1773	1265

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 14, 2001	0.1	Original	22

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